AIRBUS GROUP INNOVATIONS

Model-based design and schedulability analysis for avionic applications on multicore platforms

Wenceslas GODARD, Airbus Group Innovations
Geoffrey NELISSEN, ISEP

AIRBUS GROUP

Ada-Europe 2016 - Industrial Workshop

Reliable Software

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Agenda

- CONCERTO (ARTEMIS project)
- Avionic concepts modeling support
- Multicore modeling support
- Partition schedule generation and response time analysis
- Experimentations
- Conclusions

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A Word on CONCERTO

"Guaranteed Component Assembly with Round Trip Analysis for Energy Efficient High-integrity Multi-core Systems"

- An ARTEMIS project, built on top of CHESS, a component-based modelling framework
- Several application domains: telecare, space, avionics, automotive, petroleum
- For the avionics use case:
  - Use of UML/MARTE profile (timing annotations)
  - Behavior description (activity)
  - Assignment to hardware
  - Response time analysis with MAST
- Ended in April 2016
- Results transferred to Polarsys ("CHESS")

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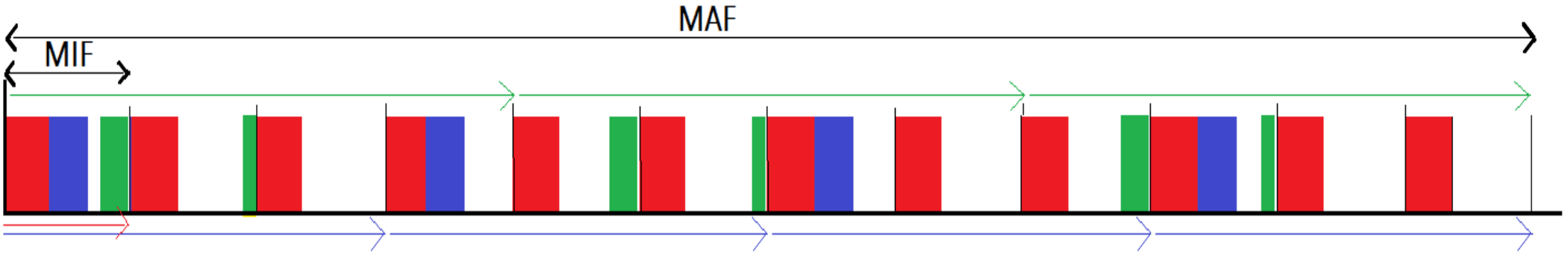
Avionic concepts

Integrated Modular Avionics (IMA) architecture

Based on robust partitioning (time, memory, IO)
With focus on timing aspects: Major and Minor Frames (MAF and MIF) for each processing unit.



P1: period = 1; P2 = period =3; P3: period =4

MIF = GCD(1,3,4) = 1
MAF = LCM (1,3,4)= 12

Avionic concepts

Definitions:

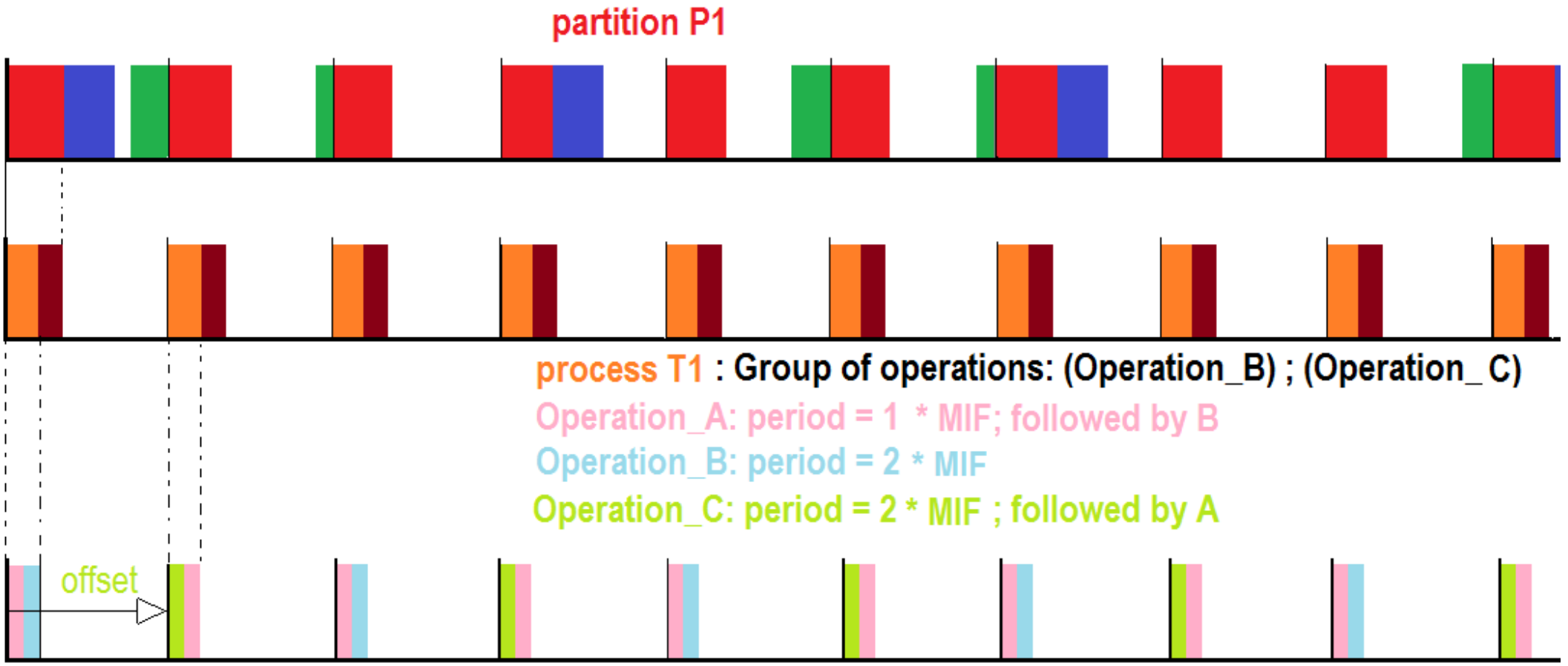
- A partition is a group of tasks (ARINC-653 processes)
- A process is composed of several functions, with optional information for exclusion relation
- An operation is related to piece of code, a function. It can have a rate and precedence constraints

Scheduling is two-level:

- Periodic and fixed at partition level (activation windows)
- Priority based at process level

Avionic concepts

Operations precedence and exclusions:



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Multicore

Pros:

Power, weight and size reduction

Cons:

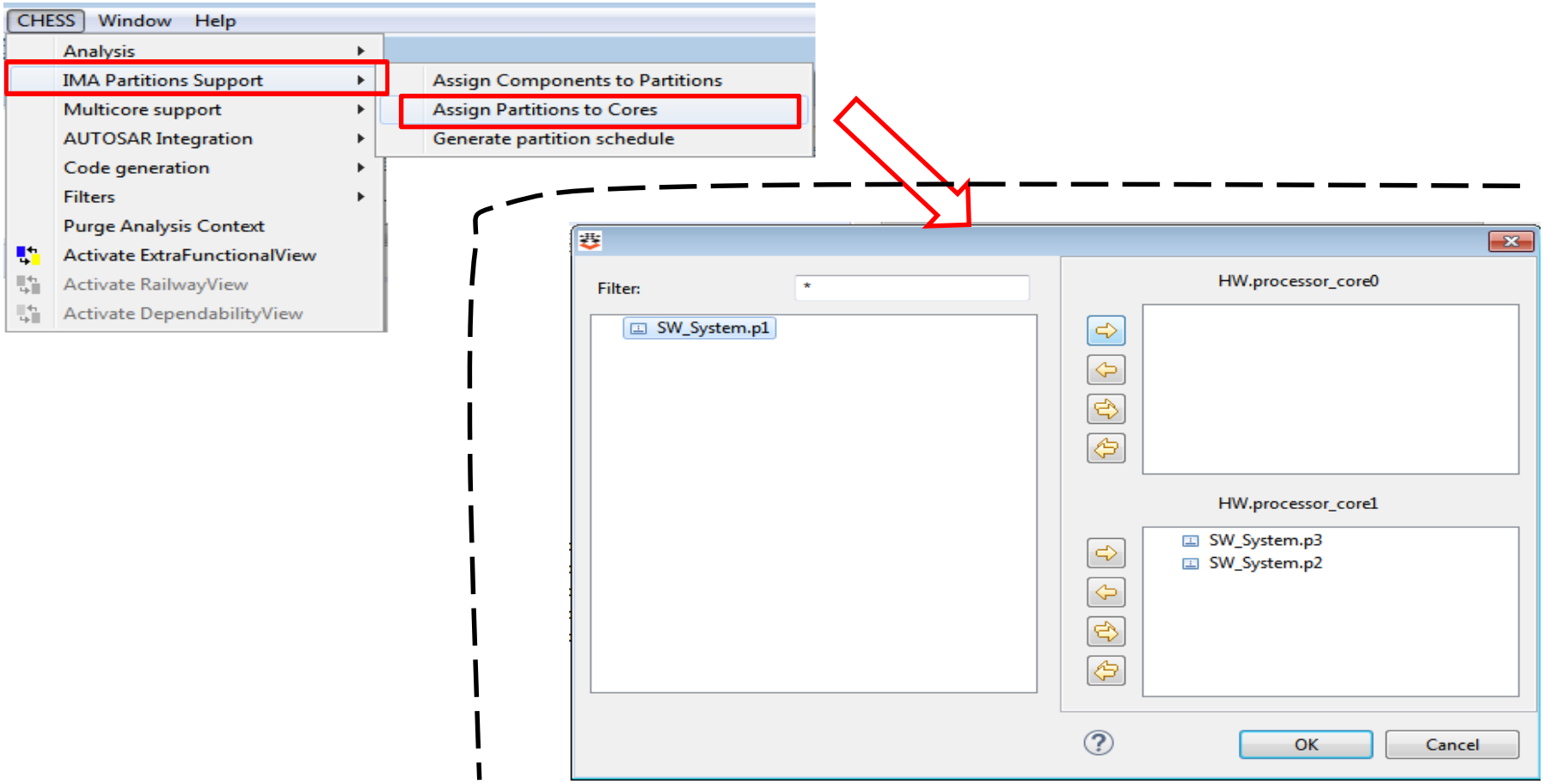
- Each core has its own partitions and schedule
- Each core interfere with each other: partitioning is broken
- Explosion of the complexity to find an optimal allocation

Solution in CONCERTO:

- Do not take into account the penalty from sharing resource (no support for interference awareness)
- Based on basic representation: number of cores. A graphical interface for static allocation of partitions to cores
- Generate partition schedules and compute response times

Multicore

Allocation of partitions to cores can be done manually…or automatically



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Schedule generation

What is generated?

	Inputs	Ouptuts
Partition	Tasks allocated; [assigned core]*	**Assigned core;** **MIF, MAF per core;** **Time-table for partition schedule (activation windows);**
Process	Period; WCET; Priority; Deadline; Group of operations	
Operation	Deadline; WCET; [following operation] Rate	**Priority;** **Phase**

Response time analysis

System is schedulable if all operations respect their deadline

Extension of MAST (http://mast.unican.es/):

- Taking into account multicore
- Model partition, processes and operations
- Transformation (to) and backpropagation (from)

Exact worst-case response time of each operation is computed

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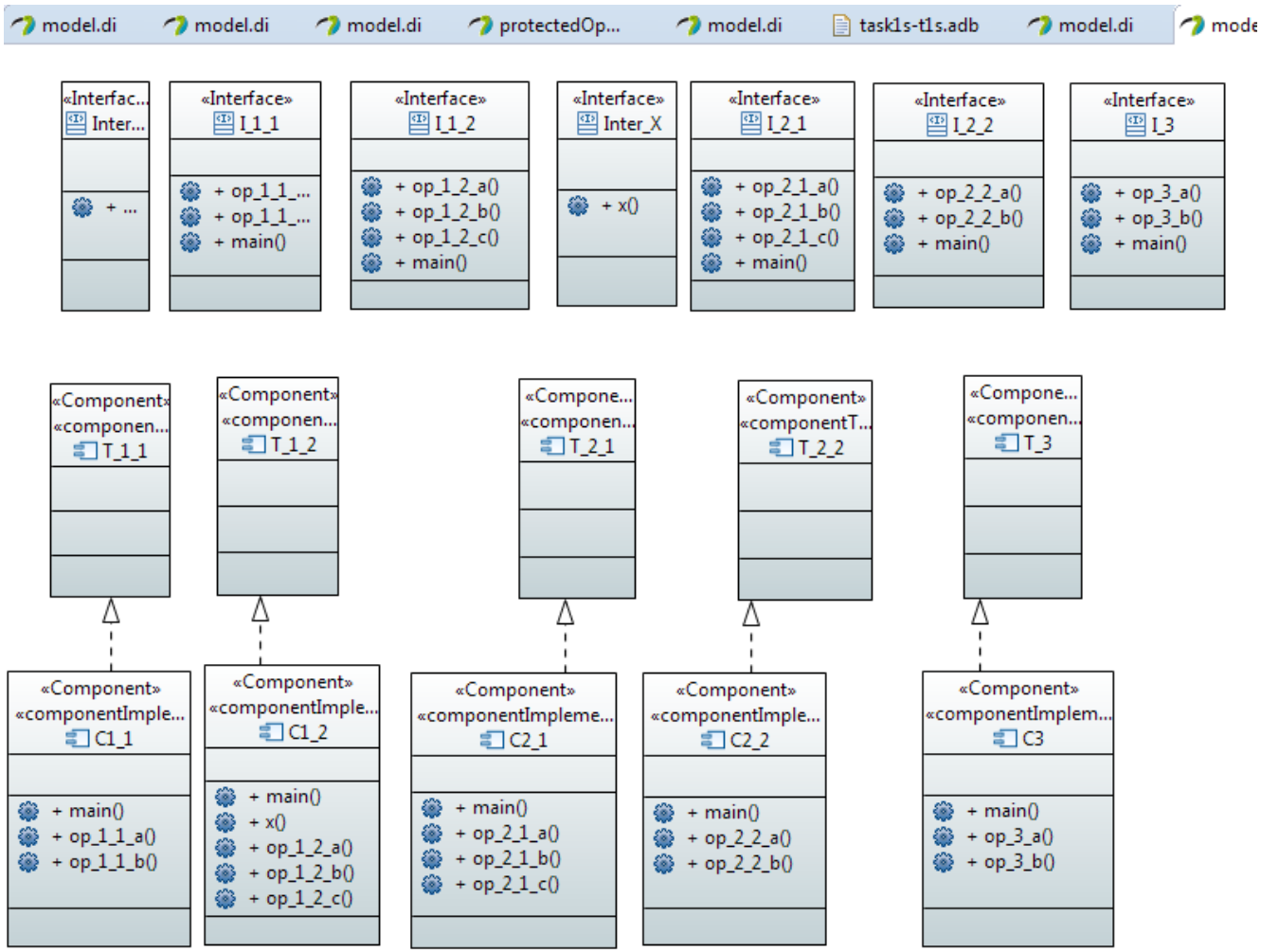
Experimentations

- Currently at research level (ARTEMIS project)
- Most input data from a real application specification – manually “extracted”
- Assumptions made on the WCET for operations and processes (no code)
- Subset implemented (tutorial is in preparation)
- Dissemination made and planned in and outside Airbus Group and its divisions

Experimentations – demo (1/6)

Definition of:

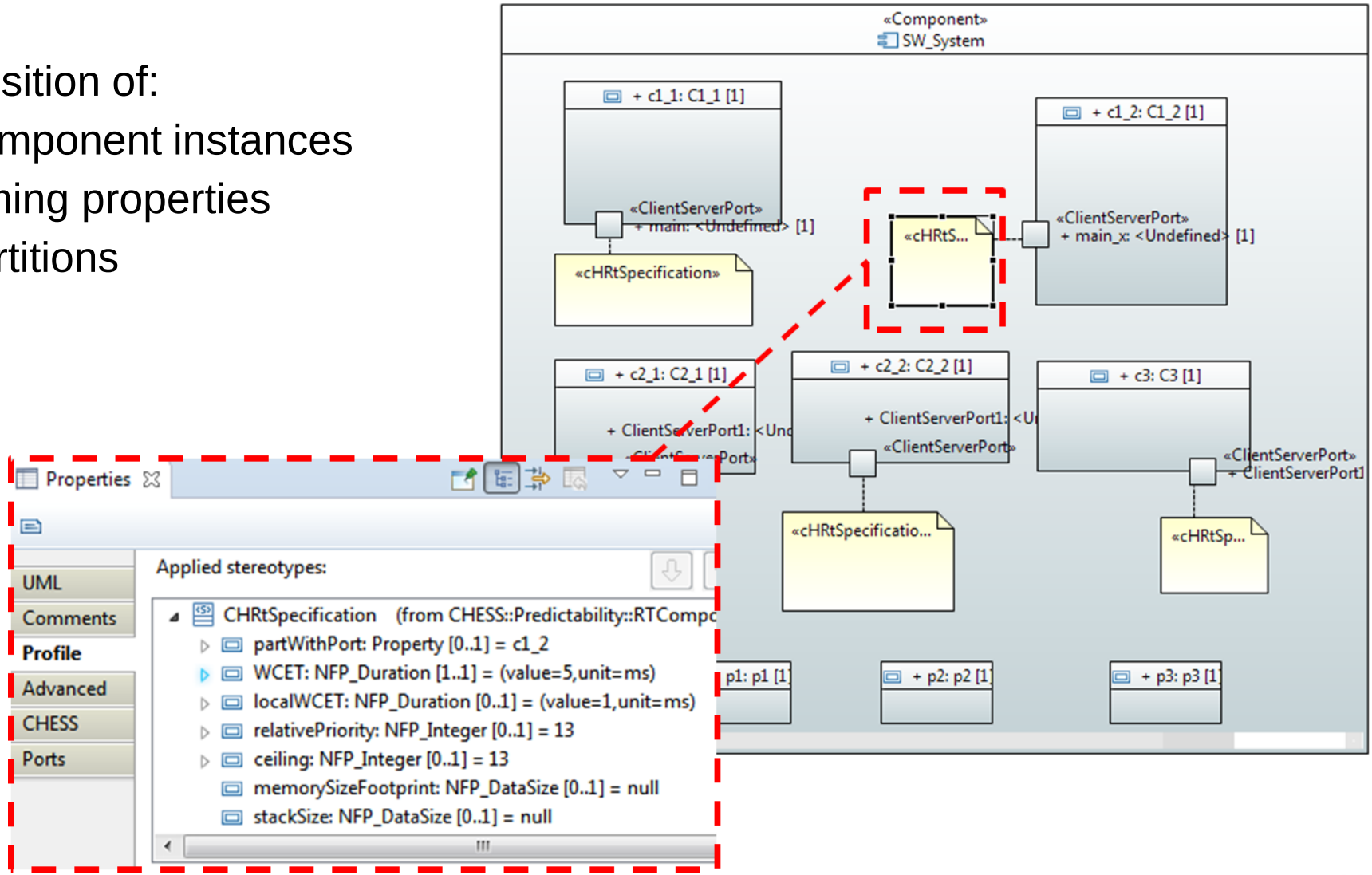
- Interfaces
- Component Types
- Component Implementations



Experimentations – demo (2/6)

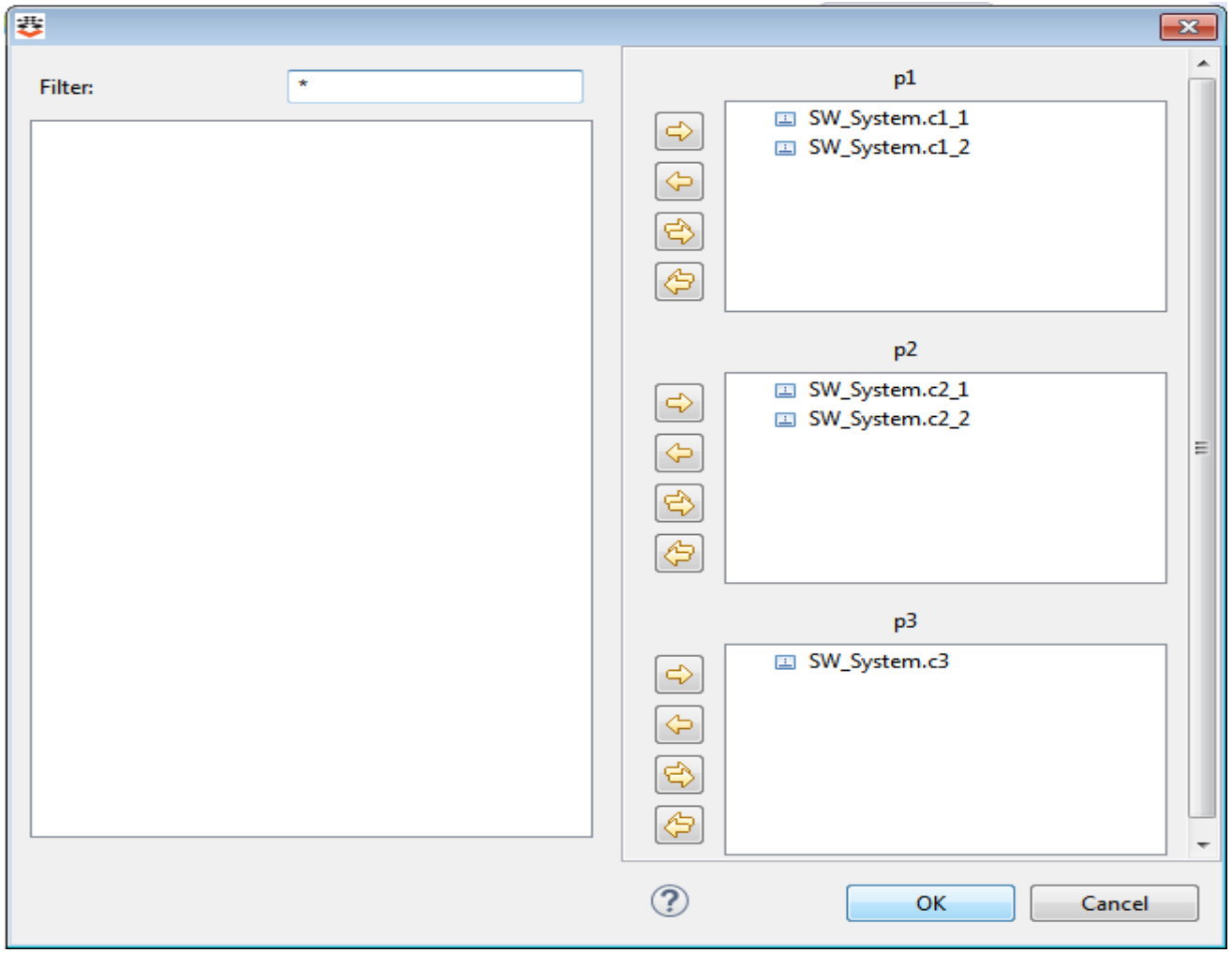
Composition of:

- Component instances
- Timing properties
- Partitions



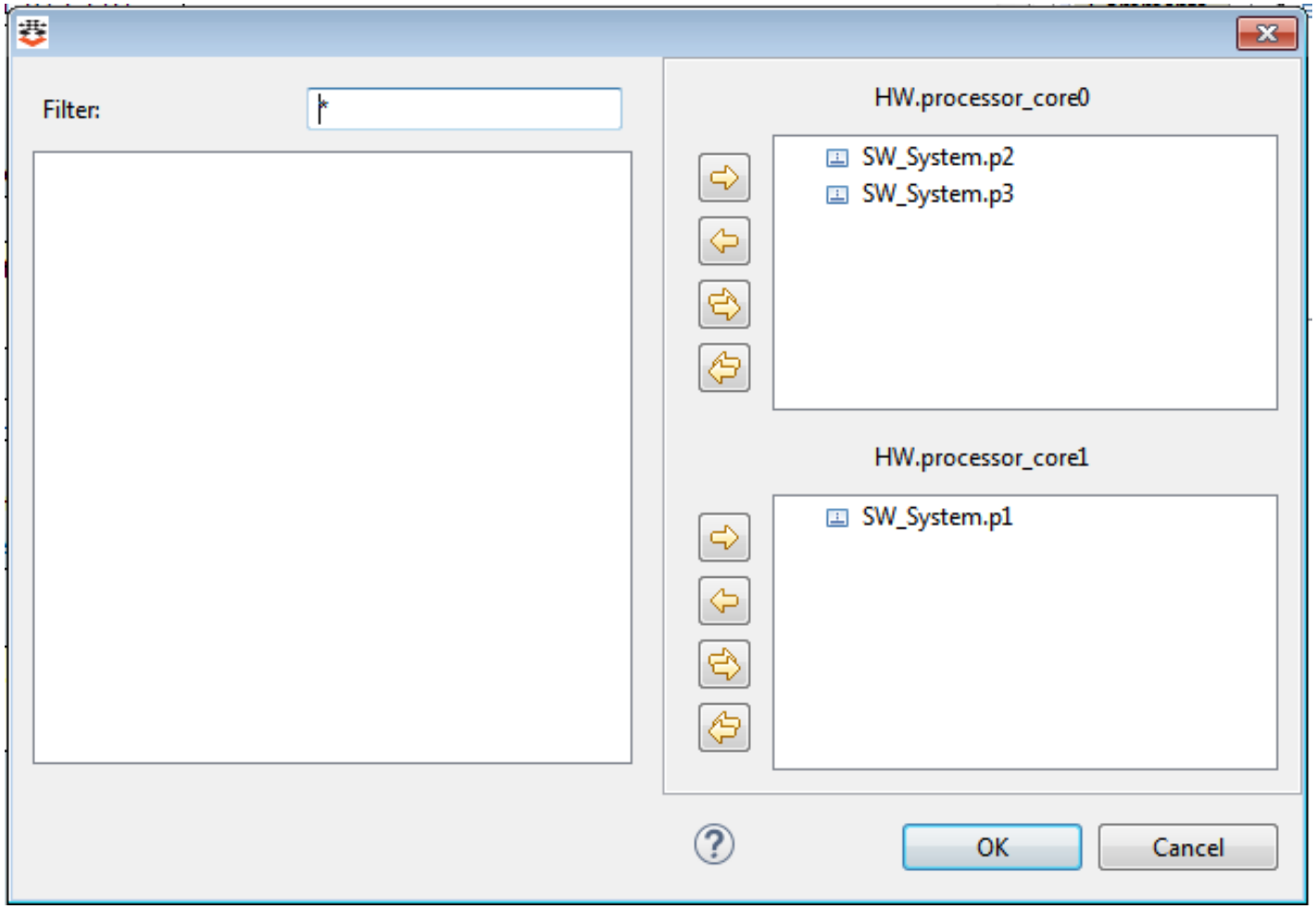
Experimentations – demo (3/6)

Assignment of Processes to **Partitions**

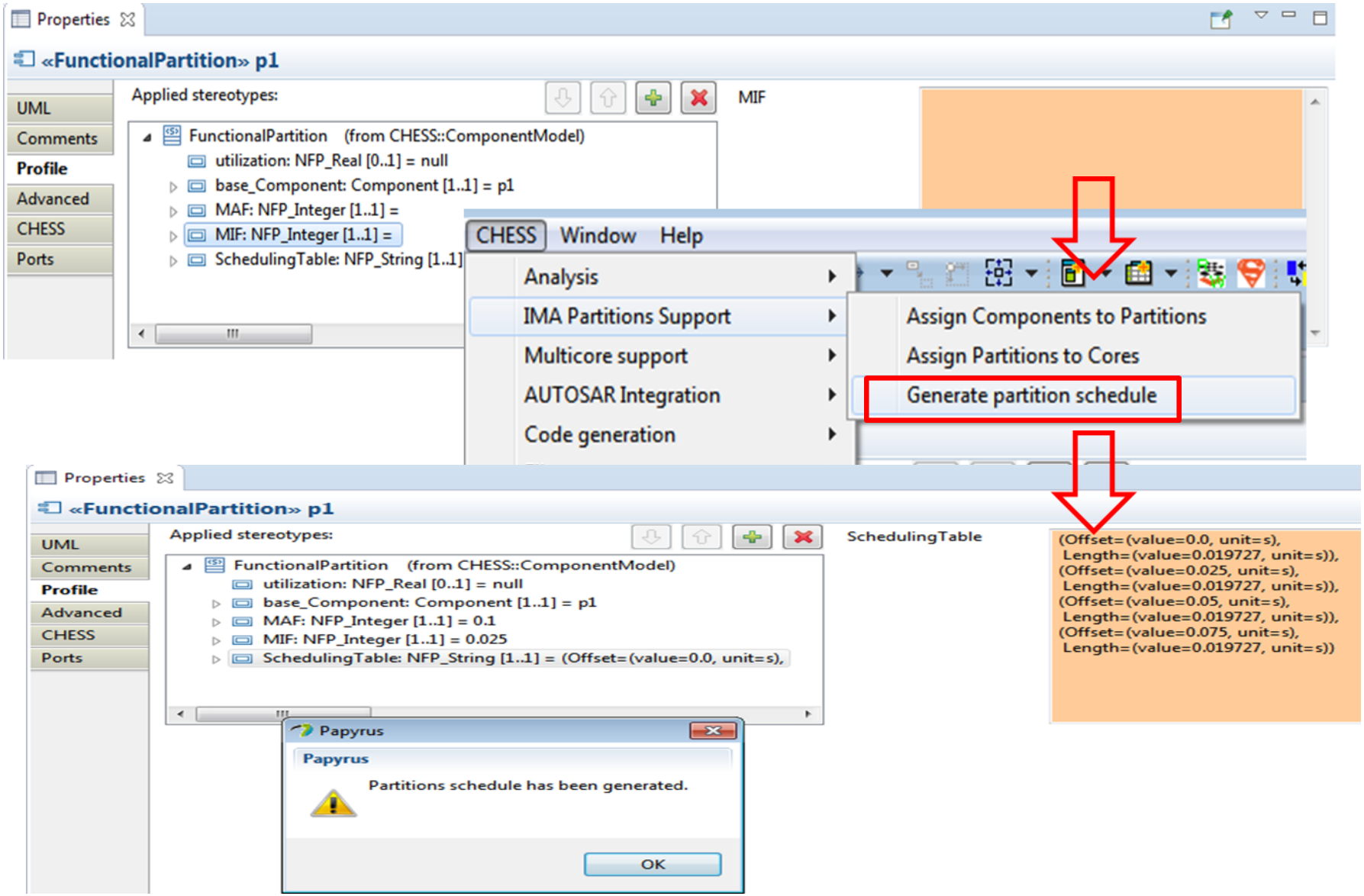


Experimentations – demo (4/6)

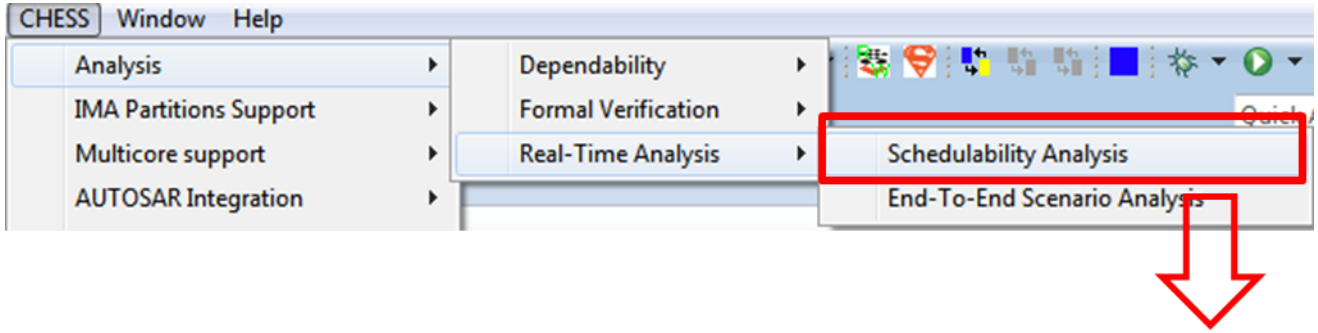
Allocation of Partitions to **Cores**



Experimentations – demo (5/6)



Experimentations – demo (6/6)



Schedulability Analysis Report

The system is schedulable

HW Instance	Utilization	Result
HW.processor_core0	64.00%	OK
HW.processor_core1	25.00%	OK

SW Instance	Operation	Response Time	Deadline	Result
SW_System.c1_1	op_1_1_a	0.079819s	0.1s	OK
SW_System.c1_1	op_1_1_b	0.039273s	0.05s	OK
SW_System.c1_2	op_1_2_c	0.001000s	0.05s	OK
SW_System.c1_2	op_1_2_a	0.003000s	0.05s	OK
SW_System.c1_2	x	0.004000s	0.05s	OK
SW_System.c1_2	op_1_2_b	0.002000s	0.05s	OK
SW_System.c2_2	op_2_2_b	0.006000s	0.05s	OK
SW_System.c2_2	op_2_2_a	0.008000s	0.05s	OK
SW_System.c2_1	op_2_1_c	0.006000s	0.05s	OK
SW_System.c2_1	op_2_1_a	0.010000s	0.05s	OK
SW_System.c2_1	op_2_1_b	0.008000s	0.05s	OK
SW_System.c3	op_3_a	0.015079s	0.1s	OK
SW_System.c3	op_3_b	0.011079s	0.1s	OK

OK Cancel

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Conclusions

Summary

Extension of CHESS environment with an extension of modelling and verification supporting IMA partitioning (SW + HW)

Includes response time analysis with backpropagation from MAST++

Formal approach, as recommended by certification authorities

Future:

Complete the modelling objects to be able to represent : ARINC-653 OS services as operations so that it can be linked with real software by code generation

Bind interference for multicore memory accesses (and caches)

Test real HW platform (ARINC-653 OS configuration according with this methodology)

Check out other use cases: http://www.concerto-project.org/

AIRBUS GROUP INNOVATIONS

Airbus Group Innovations (Head Offices)

Willy-Messerschmitt-Straße
85521 Ottobrunn
Germany

12 rue Pasteur – BP 76
92152 Suresnes cedex
France

www.airbus-group.com

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