SEVENTH FRAMEWORK PROGRAMME

PROXIMA

Multi-Core Platforms for Mixed-Criticality Systems: The PROXIMA Approach

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Challenges and new Approaches for
Dependable and Cyber-Physical Systems Engineering

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PROXIMA. Who are we?

Probabilistic real-time control of mixed-criticality multicore and manycore systems (PROXIMA)

Coordinator: Francisco J. Cazorla (BSC)

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Integrated Project (IP), Budget total: 6,793,991 Euro

Barcelona Supercomputing Center
Rapita Systems Limited
Sysgo S.A.S
Universita Degli Studi Di Padova
INRIA
Aeroflex Gaisler Ab
Airbus Operations SAS
University of York
Airbus Defence and Space
IKERLAN S.COOP
Infineon Technologies UK Ltd

PROXIMA Consortium

Why is PROXIMA?

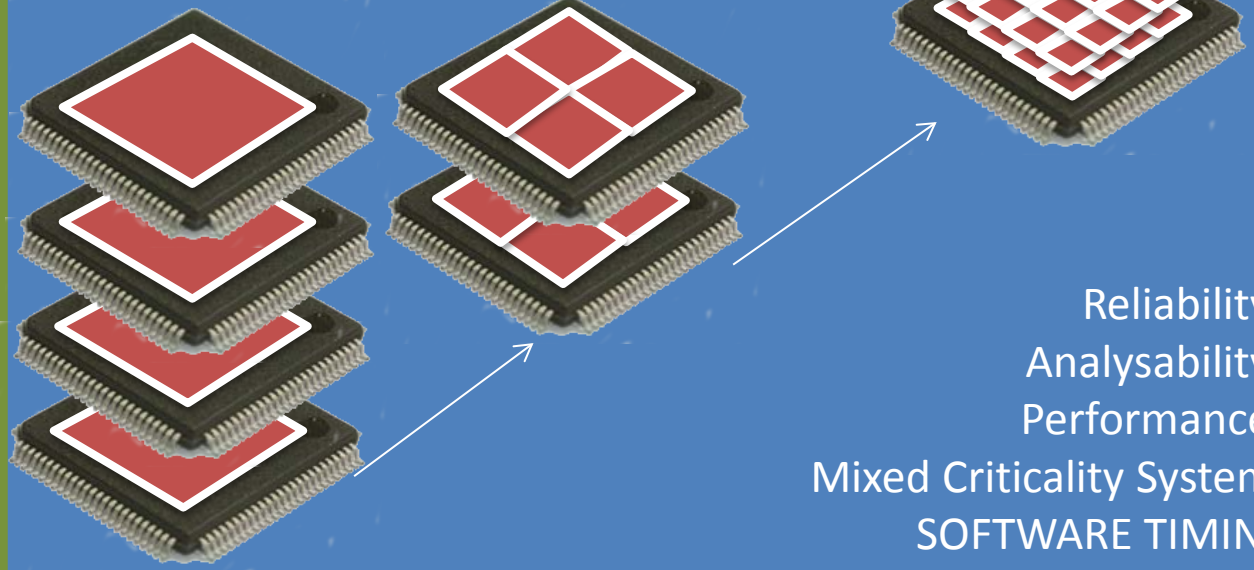
Critical Real-time Embedded Systems

Capability

Single Core

Multi Core

Many Core



Reliability?
Analysability?
Performance?
Mixed Criticality Systems
SOFTWARE TIMING

Aerospace

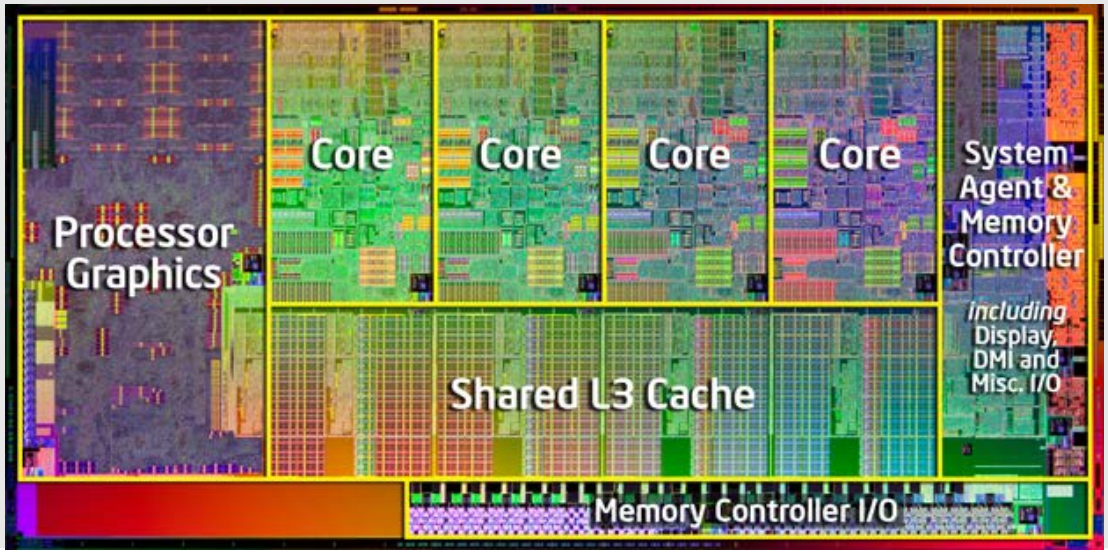
Automotive

Space

Rail

Deterministic Modelling

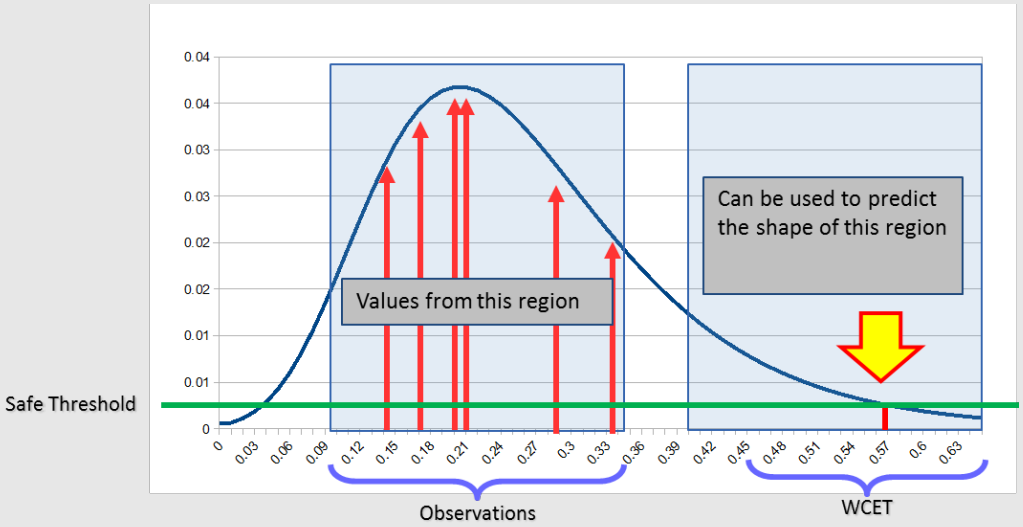
- Time Analysability ⟷ Time Determinism
  - *Current approaches rest on determinism* to achieve analysability
  - Approach: For a given input set and system state, use a causal model to derive the new system state and the associated timing
    - System state → event → new system state
- Possible in the past with simple HW/SW
  - the use of more complex HW/SW makes this approach impractical

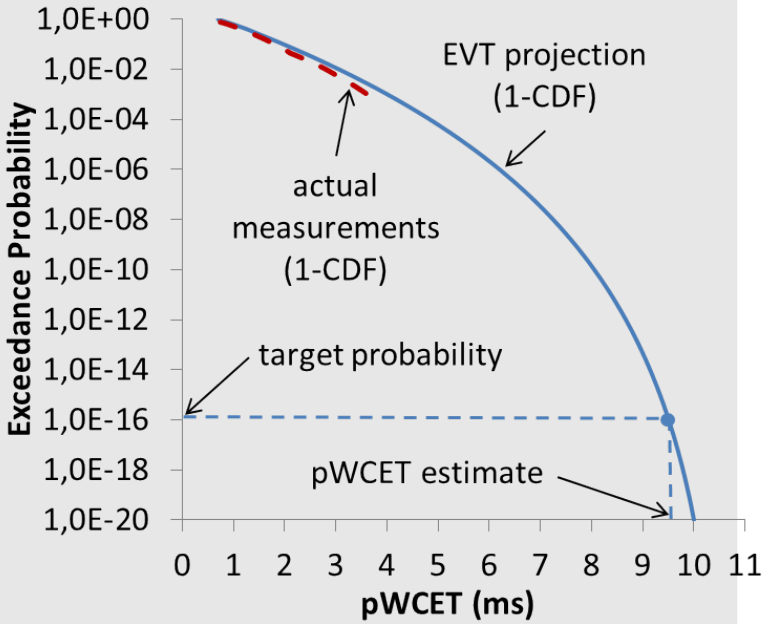


Probabilistic Modelling

- Approach:
  - Replacing deterministic approaches with probabilistic ones
    - Probabilistic analysis
  - Get rid of the need (and cost) of the detail design knowledge required to causally model the timing behavior of all system resources of interest.
- Principle: Randomise resource timing behaviour
  - Make resource latency accurately captured with a probabilistic law
- Benefit:
  - The intrinsic complexity of novel multicore and manycore processor architectures naturally becomes treatable by probabilistic timing analysis.
- **Functional behaviour is left unchanged**

Measurement Based PTA





MBPTA

- Collect some measurements (few)
- Apply probabilistic methods (e.g., Extreme Value Theory)
- pWCET estimates for arbitrarily low probabilities

Benefits

- Allows the measurement of WCET with a given level of confidence, rather than a more heuristic overhead
- pWCET are competitive with regard to existing techniques

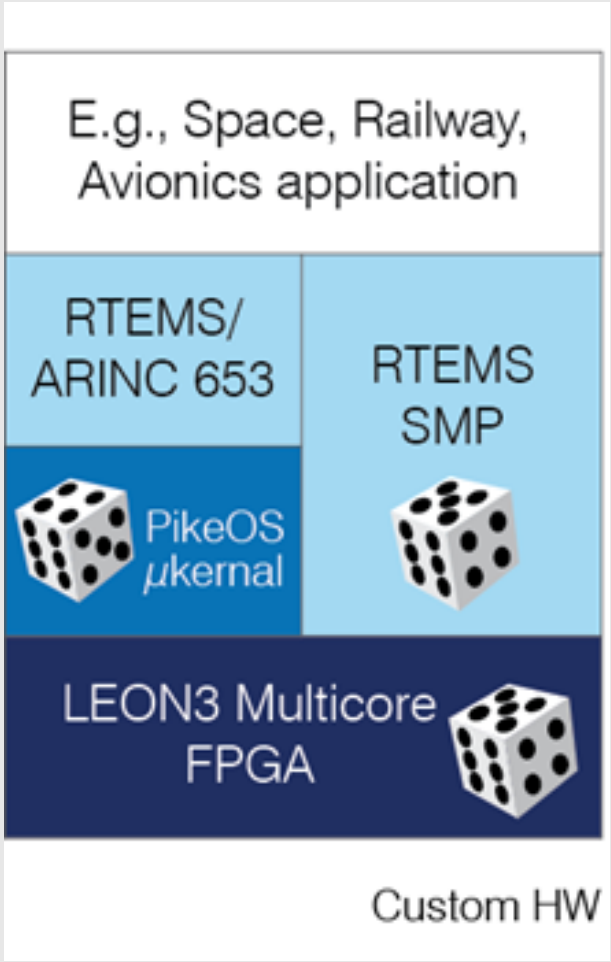
Myths

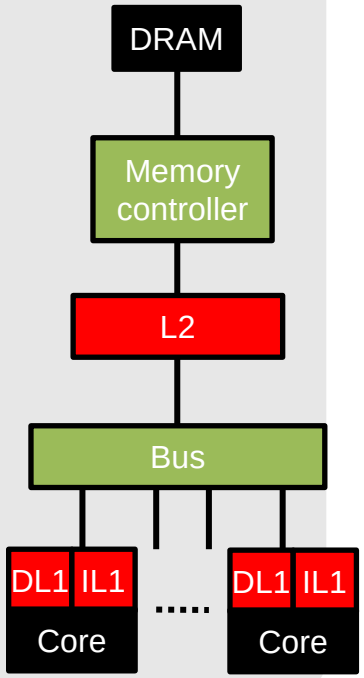
- Need to ‘re-randomise’ most hardware resources WRONG!
  - “Whatever solution makes a hw/sw component analysable with STA/MBTA makes it also analysable with SPTA/MBPTA”
    - Bus arbitration: TDMA → PTA analysable
  - PTA focuses on those resources with high jitter that are hard to track with STA/MBPTA
- Use branch hit/miss frequency as probabilities WRONG!
  - PTA techniques are made branch aware
  - The pWCET obtained does not depend on frequency of branches
    - Recall, branches have an associated frequency NOT probability

PROXIMA Multicore Platforms

Muliticore on FPGA + industrial tool chain

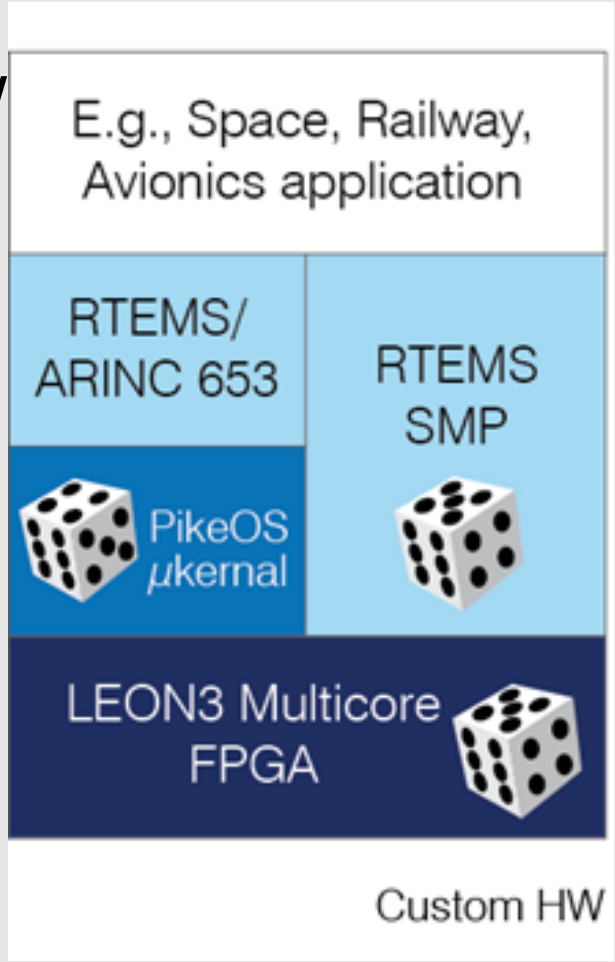
- Leon3-based SoC on a Terasic DE4 board
  - 4-LEON3 cores
    - private Icache and Dcache; instruction and data TLBs; in-order pipeline
    - Shared on-chip L2 cache through a shared bus
  - Shared memory controller and off-chip bus
- RTOS (Time compos.)
  - Baremetal, PikeOS and RTEMS
- RapiTime

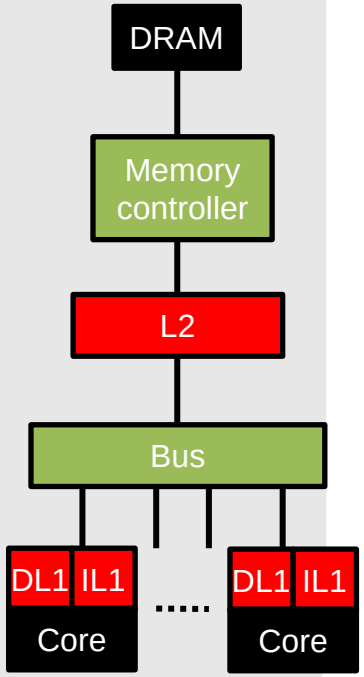




Muliticore on FPGA + industrial tool chain

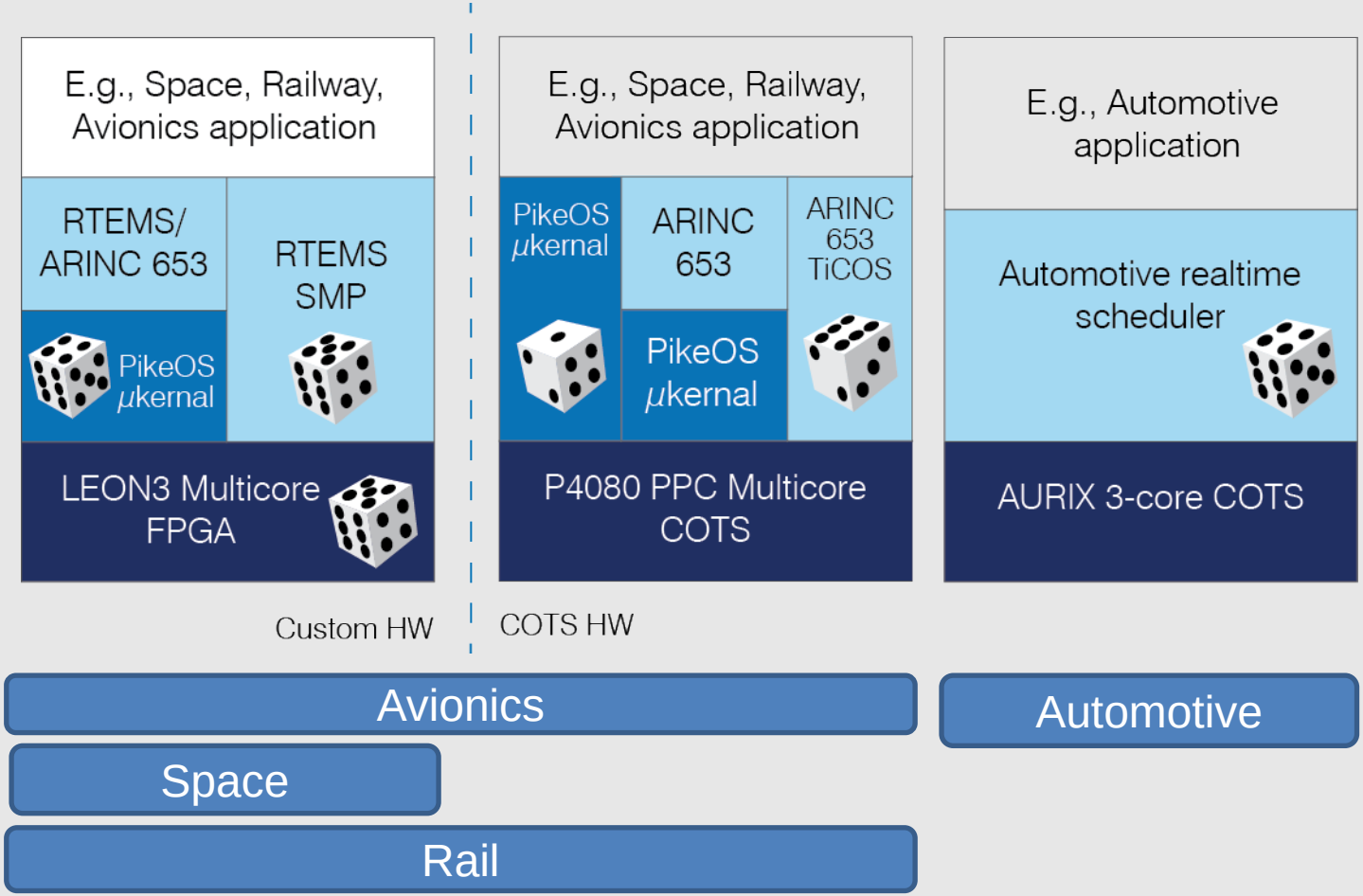
- HW randomisation will be developed making the HW fully PTA-compliant
  - Bus and memory controller
    - Random permutations
  - Caches
    - Random placement and random replacement
  - At core level
    - Response on longest latency for the FPU





COTS Multicore

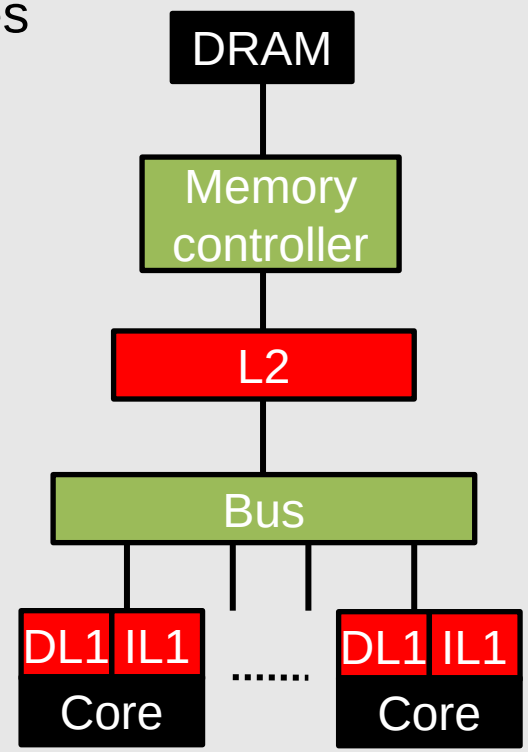
- From HW randomisation to SW randomisation



Multicore: An avionics case study

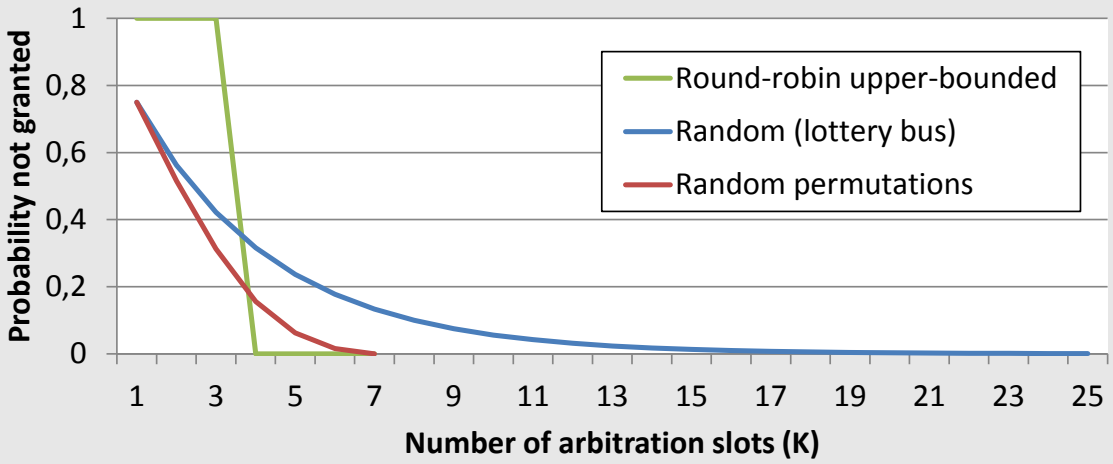
Challenges

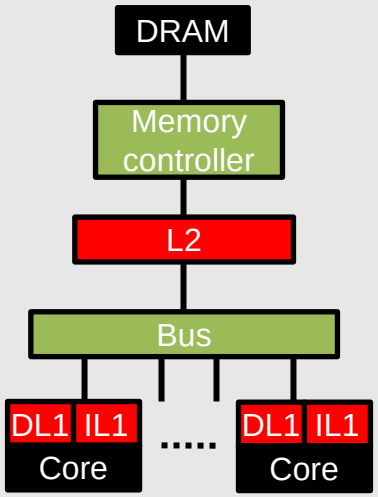
- Multicore bring many challenges to real-time system design and deployment
- Our focus: contention interference
  - Jitter that application suffers due to the load that it contender application put on hardware shared resources
- Goal: time composability
  - pWCET derived for a task should not depend on its co-runners
- Reference architecture:
  - Bus
  - Memory controller
  - L2 cache → partitioned



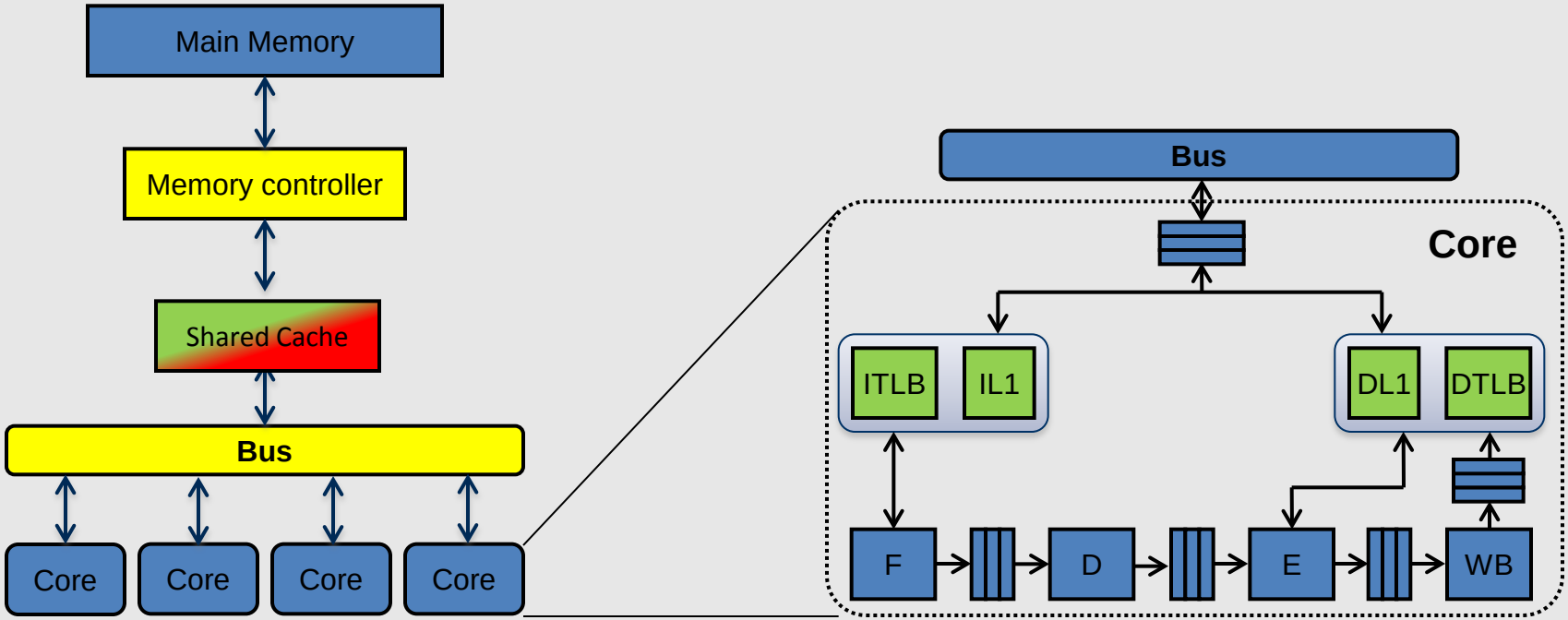
Arbitration policies

- Used for the **bus** and **memory controller**
- Probabilistically bound effect of inter-task interferences
  - **Round Robin***
  - **Random (lottery):** Select randomly the bus access slot
  - **Random permutations:** Random bus access slot permutation are generated for all contenders
    - At analysis time, always **assume the maximum number of contenders**





Avionics Case Study: HW Setups



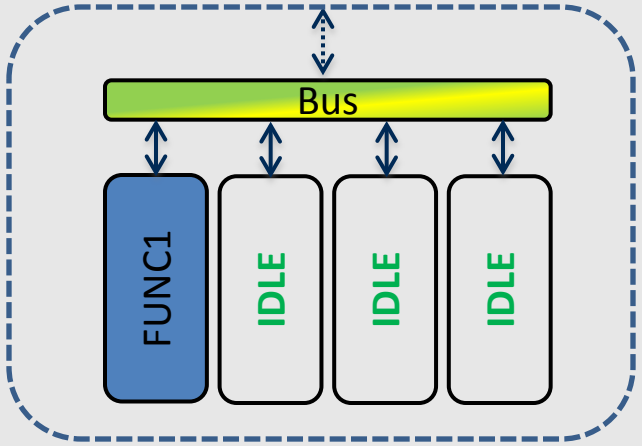
Deterministic

- MOD / LRU
- Round Robin
- Columnization

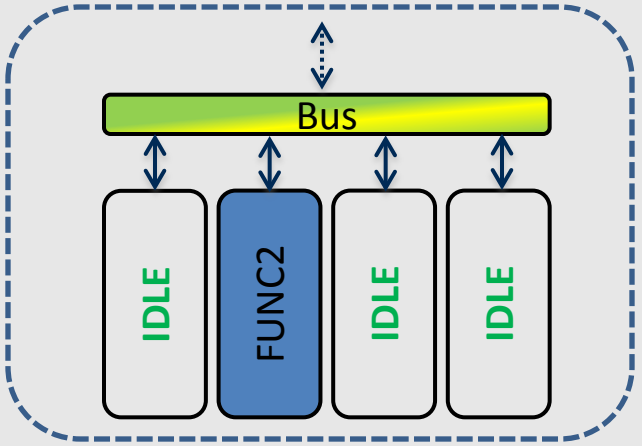
PTA

- RP / RR
- Random Permutations
- Columnization

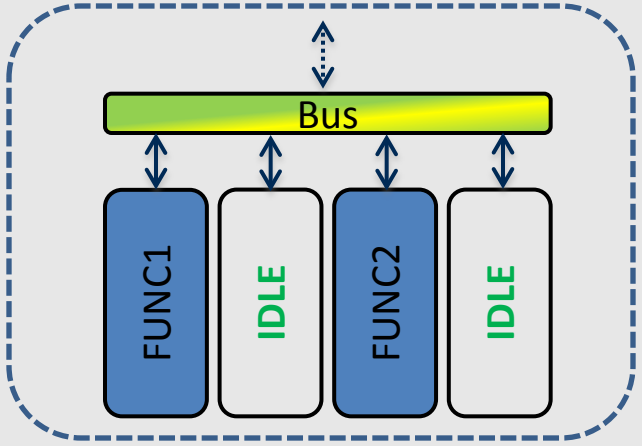
Avionics Case Study: Application Setup



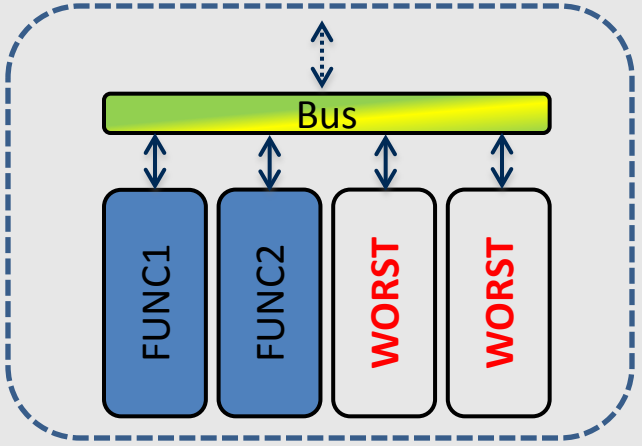
FUNC1_ALONE



FUNC2_ALONE

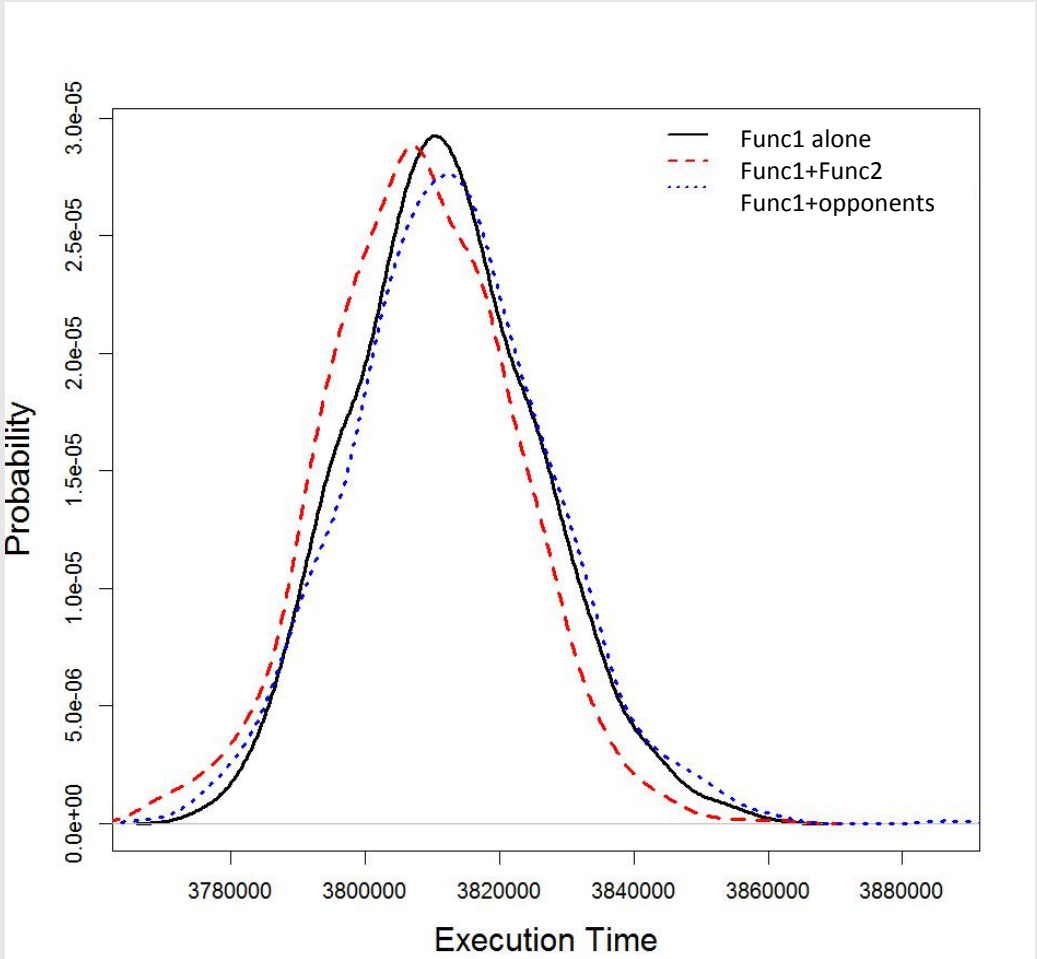


FUNC1+FUNC2_IDLE



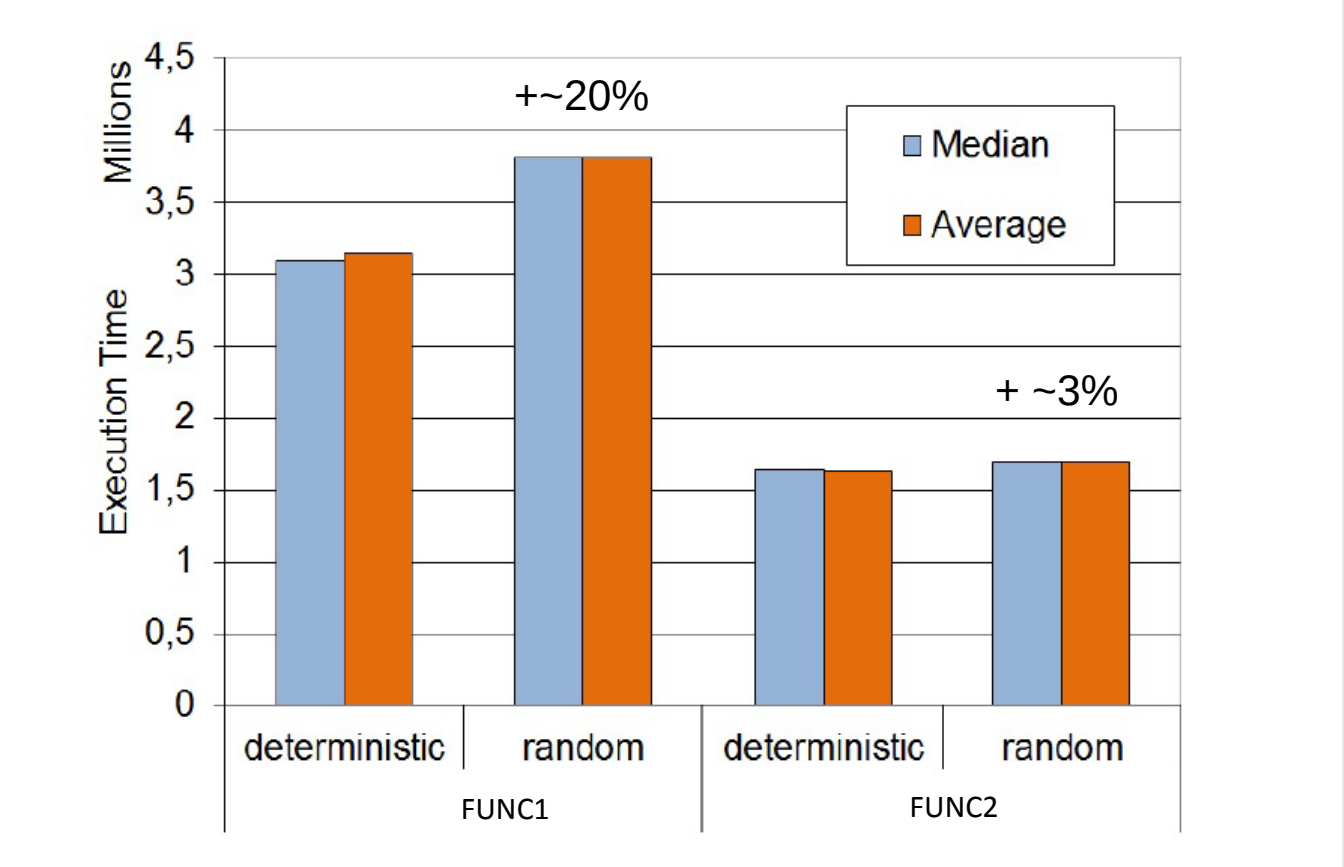
FUNC1+FUNC2_WORST

Avionics Case Study: Composability



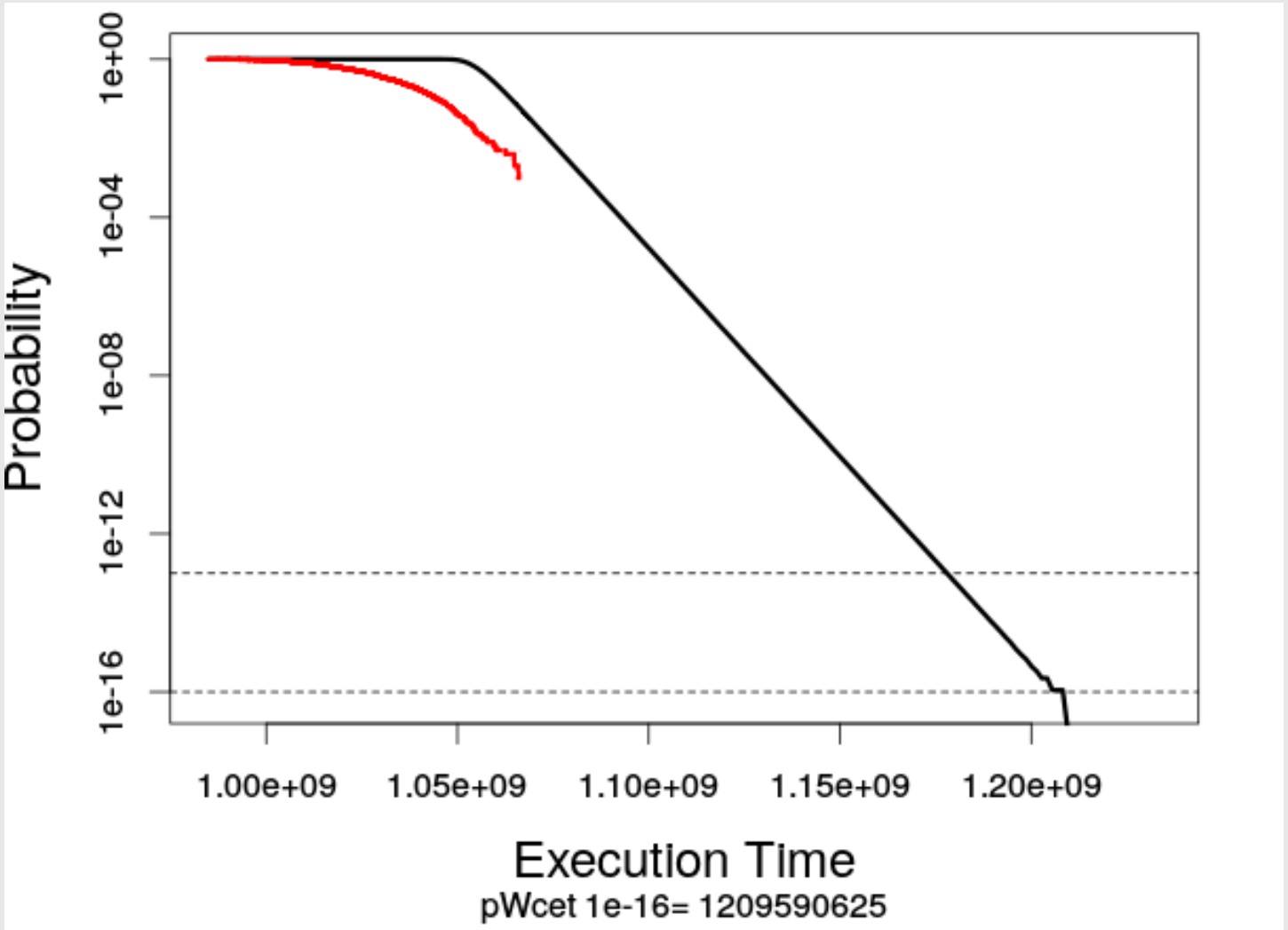
Observed execution time density functions of the application under analysis, i.e. FUNC1 when executing on the PTA multicore processor under different workloads: independent of other applications

Avionics Case Study: Average Perf.

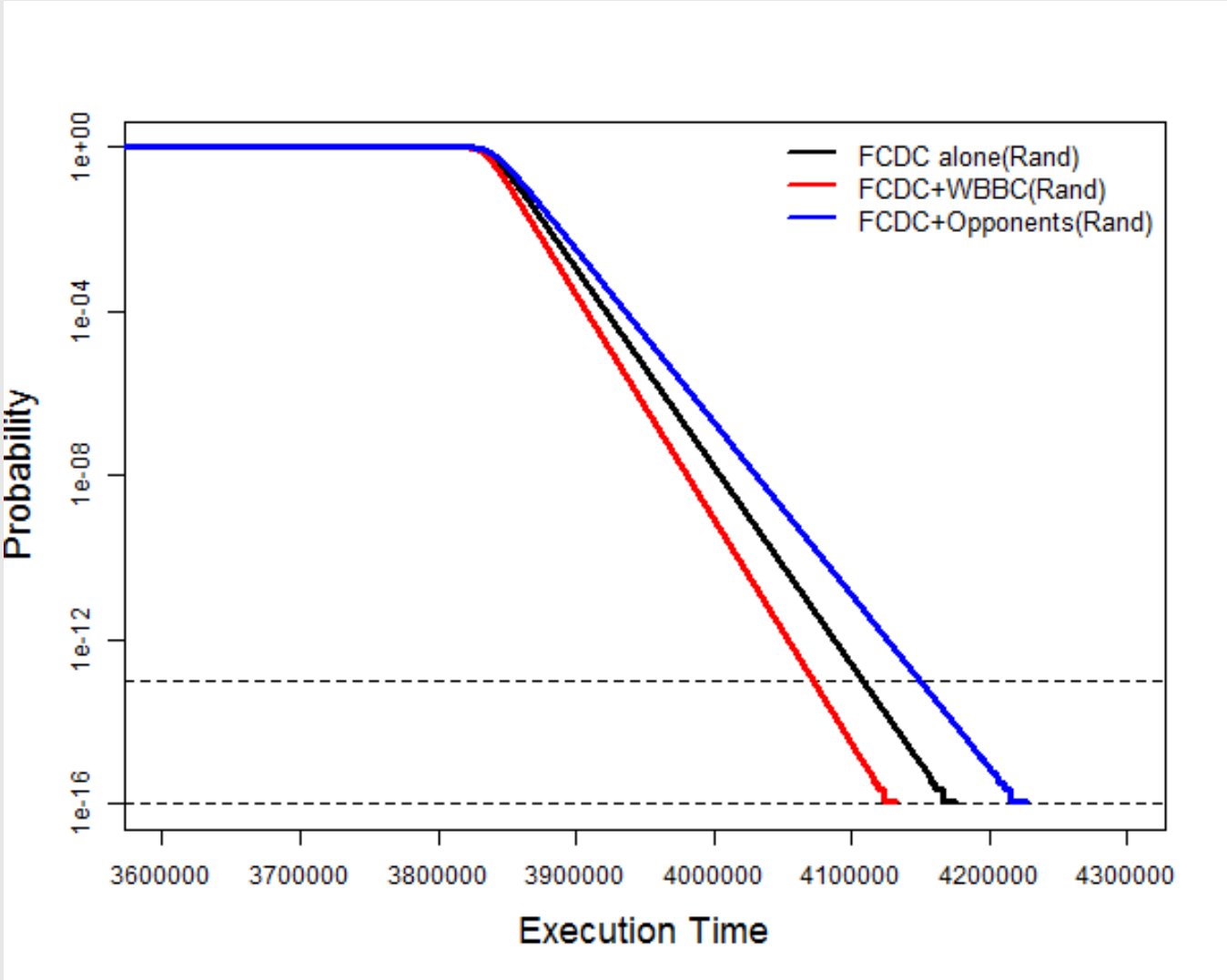


Average and Median of execution times of FUNC1 and FUNC2 on the randomised and deterministic architecture

Avionics Case Study: pWCET estimates



Avionics Case Study: pWCET estimates



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