CISTER
Research Centre in
Real-Time & Embedded
Computing Systems

Guest Editorial

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CISTER-TR-181111

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Abstract

Real-Time Systems (2018) 54:797–799
https://doi.org/10.1007/s11241-018-9317-8

Guest editorial: real-time networks and systems

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Published online: 4 September 2018

This section of *Real-Time Systems* provides extended journal versions of the outstanding work presented at the 24th International Conference on Real-Time Networks and Systems (RTNS 2016), held at Université de Bretagne Occidentale (November 2016, in Brest, France). The purpose of RTNS is to provide a venue for sharing new ideas, experiences and information among academic researchers, developers and service providers in the field of real-time systems and networks. The 24th edition of the conference continued the established series with a rich program of 34 papers (out of 75 submissions), with a diversity of topics, such as transactions and distributed systems, network analysis, synchronous dataflow graphs, scheduling and schedulability, periodic systems and control, network optimization, many-core and networks-on-chip, multicore scheduling, timing analysis, parallelism, a clear demonstration of the broad scope of real-time systems and networks research. The special issue consists of four papers that cover various areas, from high level system design and optimization to low level timing analysis of computer systems and networks, which have undergone a rigorous peer-review process according to the journal's high standards.

The first paper "A Design Flow for Supporting Component-based Software Development in Multiprocessor Real-Time Systems", written by Alessandro Biondi, Giorgio Buttazzo and Marko Bertogna, presents a design flow for component-based development on multiprocessor platforms, using Mixed-Integer Linear Program (MILP) formulations. The proposed methodology first addresses the problem of partitioning applications into virtual processors using reservation servers, and then a second method to allocate virtual processors to physical processors, both taking resource sharing into account. The methodology is evaluated both in terms of schedulability as well as run-time of the optimization problem.

The second article "Optimal Harmonic Period Assignment: Complexity Results and Approximation Algorithms", written by Morteza Mohaqeqi, Mitra Nasri, Yang Xu, Anton Cervin, and Karl-Erik Årzén, is about the design of digital control systems, where the period of tasks can be chosen within a certain range without impairing the

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performances. Focus is on allocating harmonic periods to tasks. The paper provides hardness results for two versions of the problem that are proved to be at least weakly NP-hard, and polynomial-time approximation algorithms for a relaxed version of the second problem. Evaluation on control systems with randomly generated plant parameters show that the relaxed problem is pertinent in terms of system design and that the approximations are efficient to maximize quality of control.

The third paper "Independent WCRT Analysis for Individual Priority Classes in Ethernet AVB", written by Jingyue Cao, Pieter Cuijpers, Reinder Bril, and Johan Lukkien, focuses on the computation of worst case response time of streams in Ethernet AVB networks. Their main contribution is an independent analysis, which relies on the sole knowledge of the properties of the stream under analysis and the priority classes enforced in the Ethernet AVB standard. This analysis targets especially complex industrial systems where the network is shared by applications developed by different parties. Authors also define conditions for which their analysis is tight, and show through experimental comparisons with state-of-the-art analysis that the benefits brought by assuming more information on the interfering streams are limited.

The issue completes with the paper "Response Time Analysis for Fixed Priority Systems with a Write-back Cache", written by Robert Ian Davis, Sebastian Altmeyer and Jan Reineke, that proposes analyses of write-back caches integrated into the response-time analysis for fixed-priority scheduling. The paper analyses different categories of write-backs, which are then integrated into state-of-the art schedulability analysis techniques for both preemptive and non-preemptive (fixed priority) systems. The paper provides an evaluation using Mälardalen and EEMBC benchmarks, comparing to no cache and a write-through cache.

We would like to thank the authors for having submitted their work to this special issue. We would also like to thank the evaluators for their time and effort in ensuring the high quality of the articles.

Sébastien Faucou has a M. Sc. (1999) in Automatic Control and Applied Informatics from École Centrale de Nantes, and a Ph. D. (2002) in Automatic Control and Applied Informatics from Université de Nantes. He is Maître de Conférences at the Institut Universitaire de Technologie de Nantes (Université de Nantes), and Permanent Member of the LS2N (Laboratory of Digital Sciences of Nantes, UMR 6004 CNRS) research unit, where he is part of the real-time systems group. His current activities are in timing analysis, run-time verification, and software engineering for dependable embedded systems. He has been General Chair of RTNS 2011 and Program Co-Chair of RTNS 2016. Since 2013 he is member of the steering committee of RTNS. Since 2017 he is Co-Chair of the High Performance Embedded Computing track of the french national group GDR CNRS SOC2.

Luís Miguel Pinho has a M. Sc. (1997) and a Ph. D. (2001) in Electrical and Computer Engineering at the University of Porto. He is Coordinator Professor at the School of Engineering of the Polytechnic Institute of Porto, and Research Associate at the CISTER (Research Centre in Real-Time and Embedded Computing Systems) research unit, where he currently leads activities in, among others, real-time parallel programming models, scheduling of real-time parallel tasks, reliable software, run-time monitoring and real-time middleware. He has participated in more than 20 R&D projects, was Coordinator of the FP7 R&D European Project P-SOCRATES and of several national projects, and CISTER coordinator and work package leader in several European and national projects. He has published more than 100 papers in international venues and journals in the area. He was Senior Researcher of the ArtistDesign Network of Excellence (NoE) and is a member of the HiPEAC NoE. He was Keynote Speaker at RTCSA 2010, General Co-Chair of ARCS 2015, and Program Co-Chair of Ada-Europe 2016 and RTNS 2016. He is Editor-in-Chief of the Ada User Journal.