Shared Resource Contention Aware Schedulability Analysis for Multiprocessor Real-Time Systems

CISTER – Research Centre in Real-Time & Embedded Computing Systems

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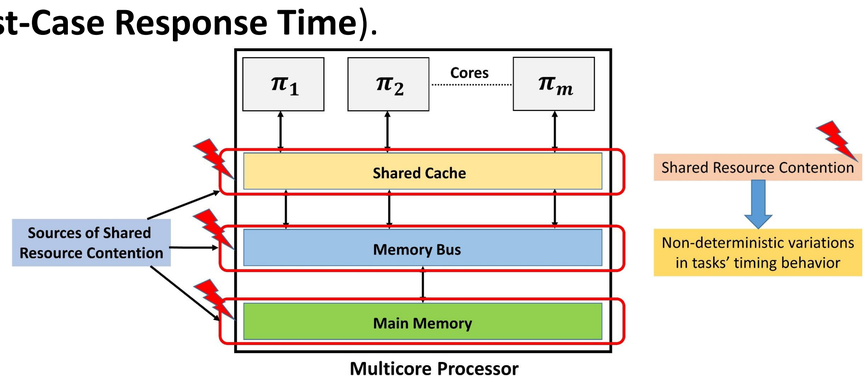
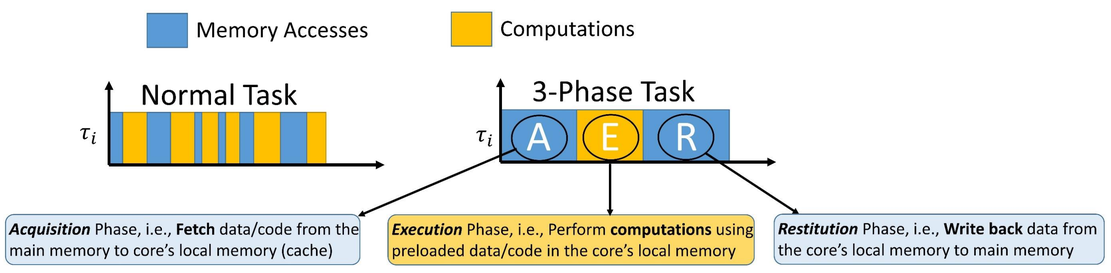
1. Motivation & Problem Definition

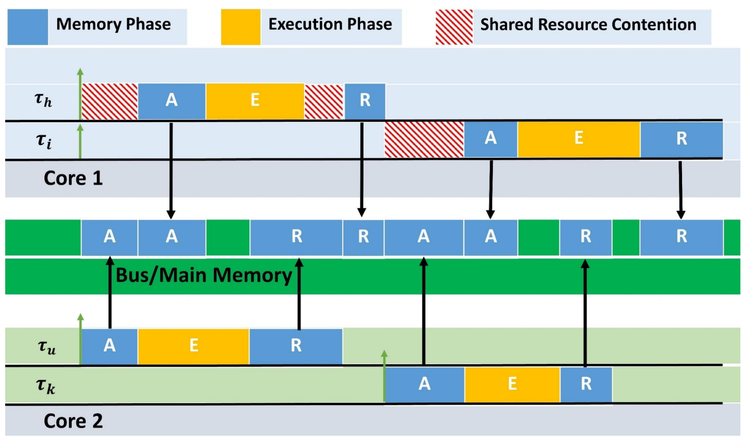
- **Shared resource contention** in **multicore** systems may lead to non-deterministic **variations** in **WCET** (**Worst-Case Execution Time**)/ **WCRT** (**Worst-Case Response Time**).



- **Dividing** the execution of **tasks** into distinct **computation** and **memory phases**, i.e., **3-phase model** [2], help **bound** shared **resource contention**.



- **3-phase tasks** can still be **subjected** to **shared resource contention** as the below figure shows.

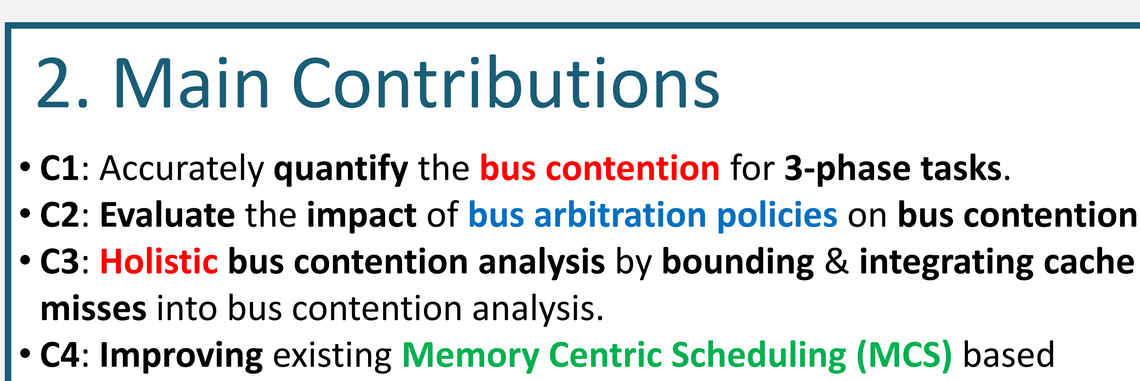


2. Main Contributions

- **C1**: Accurately **quantify** the **bus contention** for **3-phase tasks**.
- **C2**: **Evaluate** the **impact** of **bus arbitration policies** on **bus contention**.
- **C3**: **Holistic bus contention analysis** by **bounding** & **integrating cache misses** into bus contention analysis.
- **C4**: **Improving** existing **Memory Centric Scheduling (MCS)** based approaches.
- **C5**: Accurately **quantify memory contention** for **3-phase tasks**.

C1: Analyzing Bus Contention

- **Job level bus contention analysis** to improve **existing task level analysis**.
- **Fine-grained analysis** using **cases/sub-cases** to emulate **different scheduling scenarios** under **FCFS bus**.
- **WCRT Analysis**= **CPU contention** + **Bus contention**

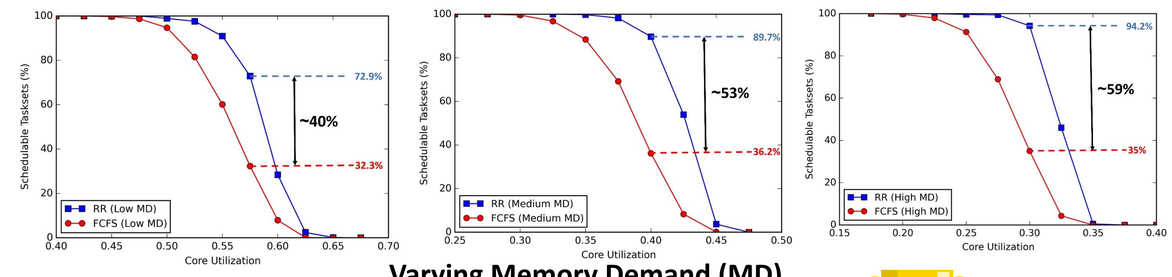


Varying Core Utilization and Number of Cores

Journal Publications: Elsevier's Journal of Systems Architecture (JSA)
Conference Publications: RTSS 2020, RTNS 2021

C2: Impact of Bus Policies

- **Evaluating** the **impact** of **bus arbitration policy** on **bus contention**.
- **Memory phase level analysis** for **Round Robin** (RR) bus.
- **Bus Contention aware WCRT analysis** for 3-phase tasks under RR bus.

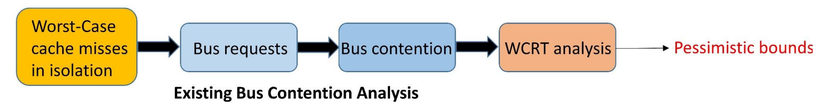


Varying Memory Demand (MD)

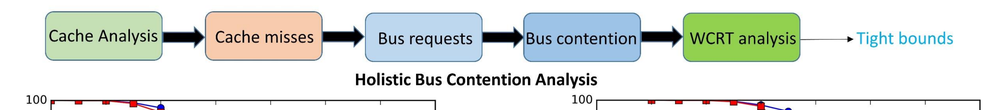
Journal Publications: Elsevier's JSA
Recipient of the **Best Paper Award** at ICESS 2021

C3: Holistic Bus Contention Analysis

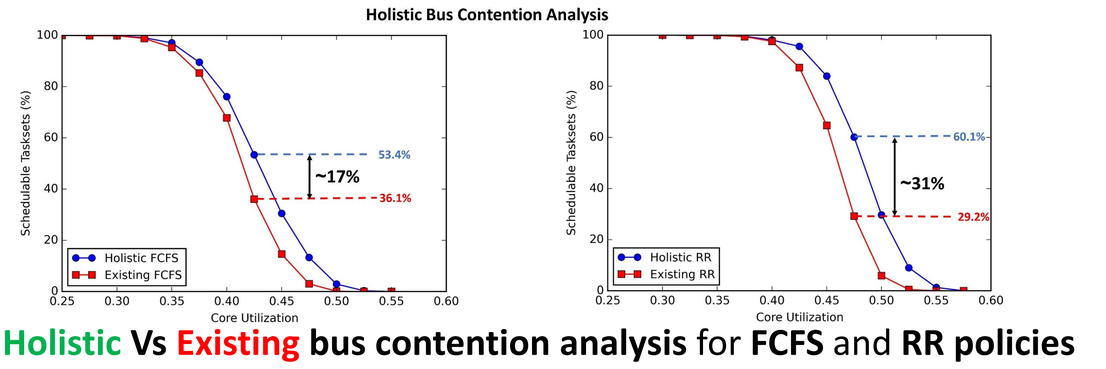
- **Overestimation** in the **number** of **bus requests** leads to **pessimistic bound** on the **bus contention**.
- **Bus contention** depends on **bus requests** which depends on **cache misses**.
- **Holistic bus contention analysis** that bounds **cache misses** to compute **bus requests** and **bus contention**.



Existing Bus Contention Analysis



Holistic Bus Contention Analysis

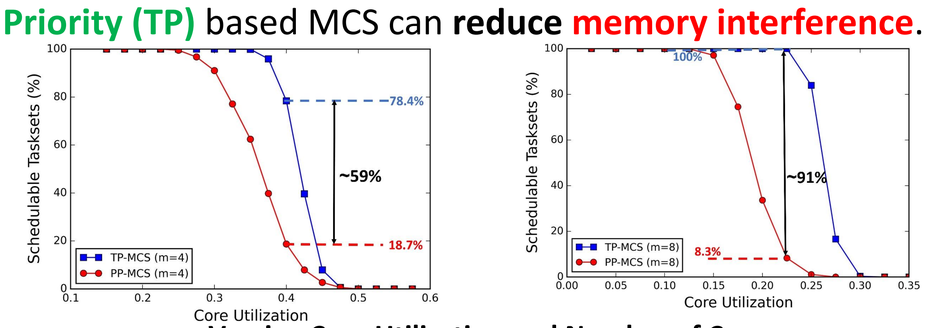


Holistic Vs Existing bus contention analysis for **FCFS** and **RR policies**

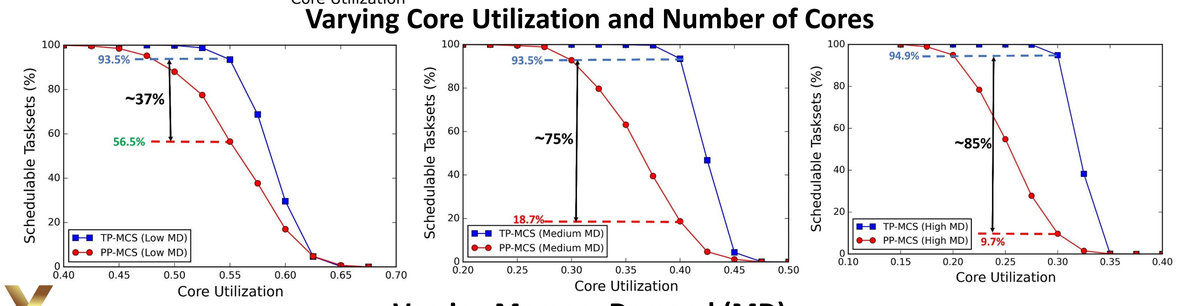
Conference Publications: RTSS 2022

C4: Memory Centric Scheduling

- Existing **Processor Priority (PP)** [1] based Memory Centric Scheduling (MCS) can **overestimate memory interference**.
- It **schedules memory phases** based on **processor priority** on which tasks execute and **ignore task priorities**.
- **Task Priority (TP)** based MCS can **reduce memory interference**.



Varying Core Utilization and Number of Cores



Varying Memory Demand (MD)

Conference Publications: RTCSA 2022

C5: Memory Contention (in Progress)

- SoA **memory contention analysis** [3] is **limited** to a certain configuration.
- It also **ignores** the **cache behavior** and **memory address mapping**.
- We are building **memory contention analysis** for **3-phase tasks** considering different **configurations** and **memory address mappings**.
- **WCRT Analysis** = **CPU contention** + **Memory contention**

References

[1] G. Schwäricke et al., "Fixed-Priority Memory-Centric Scheduler for COTS-Based Multiprocessors", ECRTS, 2020.

[2] G. Durrieu et al., "Predictable Flight Management System Implementation on a Multicore Processor", ERTS'14, 2014.

[3] D. Casini et al., "A Holistic Memory Contention Analysis for Parallel Real-Time Tasks under Partitioned Scheduling" RTAS 2020.

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