parMERASA

Universität Augsburg University

Experiences and Results of Parallelisation of Industrial Hard Real-time Applications for the parMERASA Multi-core

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Joint paper on parMERASA Project Results

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parMERASA

Multi-Core Execution of *parallelised* Hard Real-Time Applications Supporting Analysability

EC FP-7 project Sept. 1, 2011 – Sept. 30, 2014
3.3 Mio EC contribution
Project webpage: http://www.parmerasa.eu

Project Partners and IAB

Universität Augsburg University

Barcelona Supercomputing Center

IRIT

technische universität dortmund

RAPITA

Honeywell

BAUER MASCHINEN

DENSO Europe

Industrial Advisory Board:

Airbus, Toulouse, France

Infineon Technologies UK Ltd, Bristol, UK

Infineon Technologies AG, Munich, Germany

BMW Group, Munich, Germany

DELPHI, Sweden

Elektrobit Automotive GmbH, Erlangen, Germany

Daimler AG, Germany

Overview

- **Motivation and Principal Objective**
- **Principal Developments and Results**
- **Parallelisation Results**
- **Conclusions**

Hard Real-time Systems

- **Hard real-time**:
  a deadline must never be missed
  if missed it may cause harm to humans or equipment

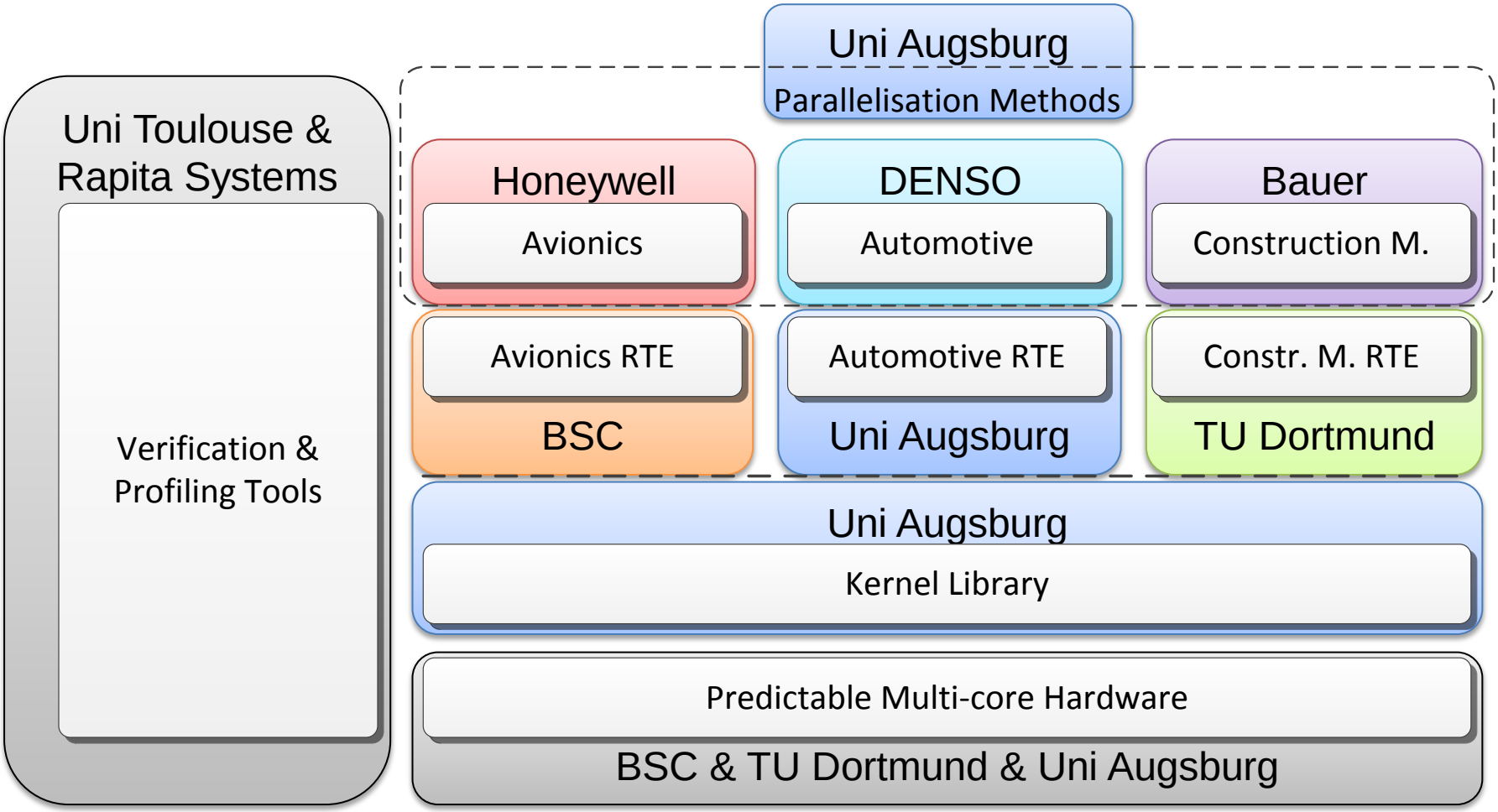
- **Mixed criticality in multi-cores**:
  combining functionalities with different levels of criticality within multi-core systems
  e.g. sub-systems to be combined that have different automotive safety integrity levels (ASIL)

Vision of parMERASA

parMERASA goes one step **beyond mixed criticality demands**:

We target future complex control algorithms by parallelising hard real-time programs to run on predictable multi-core processors.

Project Layout



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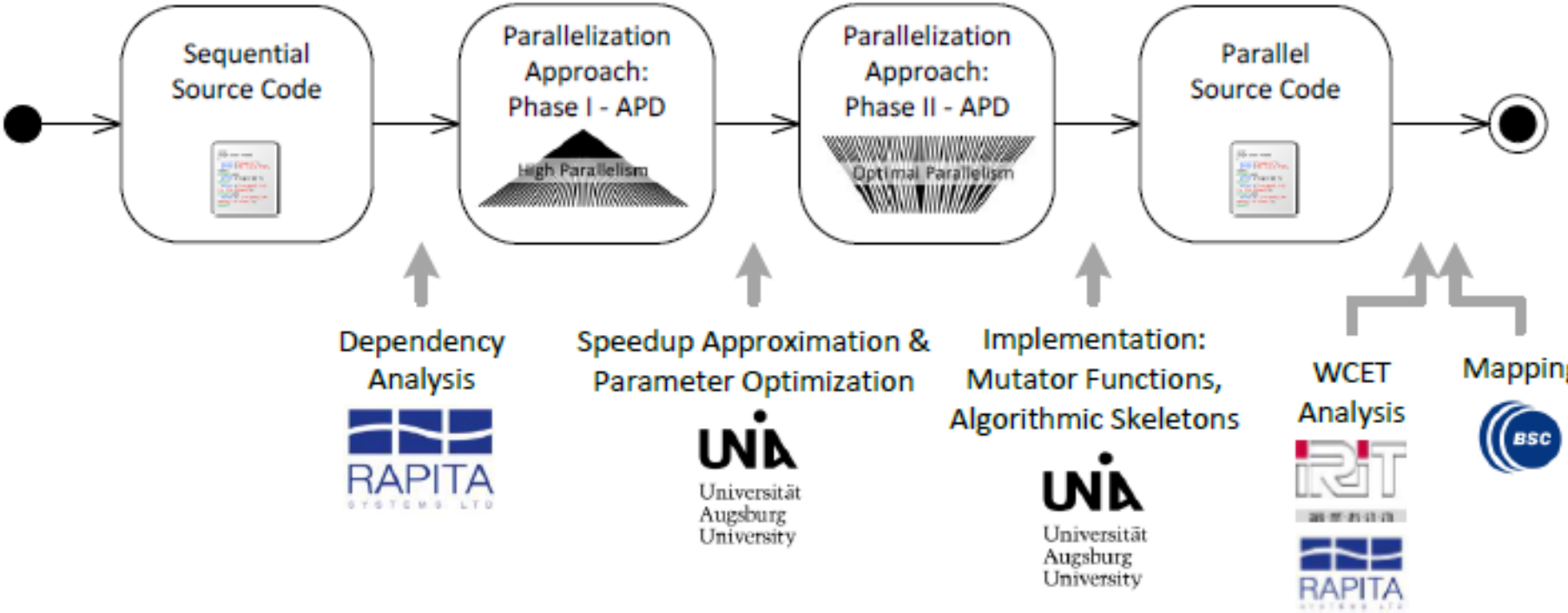
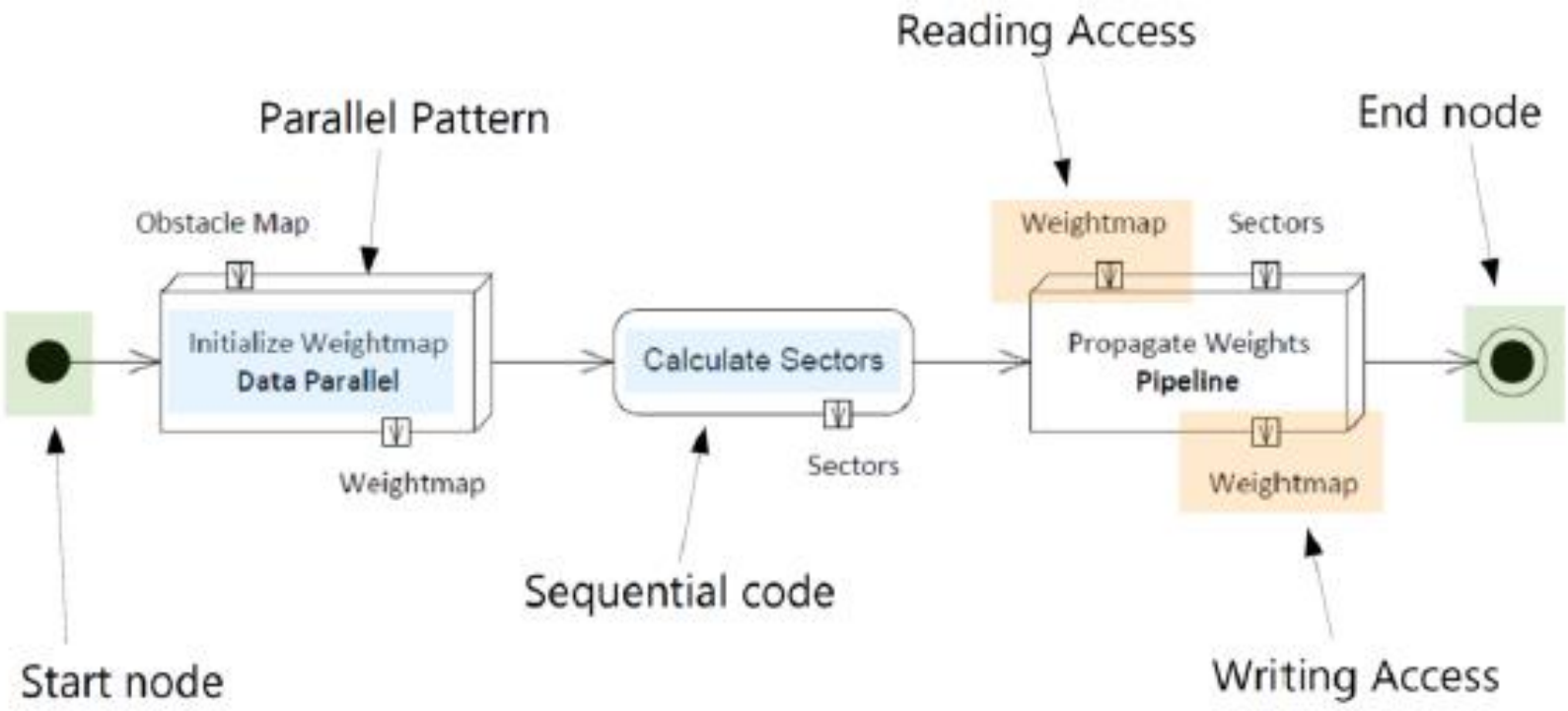
Principal Results (1)

- Pattern-based approach to efficiently parallelise industrial applications for embedded real-time systems.



Principal Results (1)

- Pattern-based approach: Activity and Pattern Diagram (ADP).



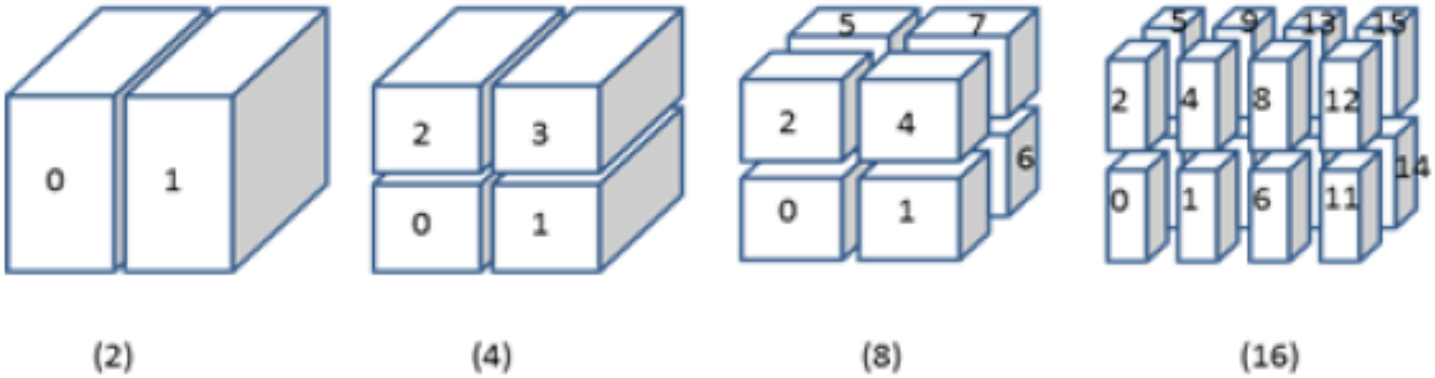
Principal Results (2): Tools

- WCET analysis and verification tools for multi-cores:
  static WCET tool OTAWA (University of Toulouse) and
  measurement-based WCET tool RapiTime
  all extended for parallel programs
- Further tools developed/extended for parallel program analysis by Rapita Systems Ltd:
  RapiTask trace viewer
  RapiCheck constraint checker
  RapiCover for code coverage
  RapiTime dependency analysis tool

Principal Results (3)

Parallelisation of four industrial hard real-time applications:

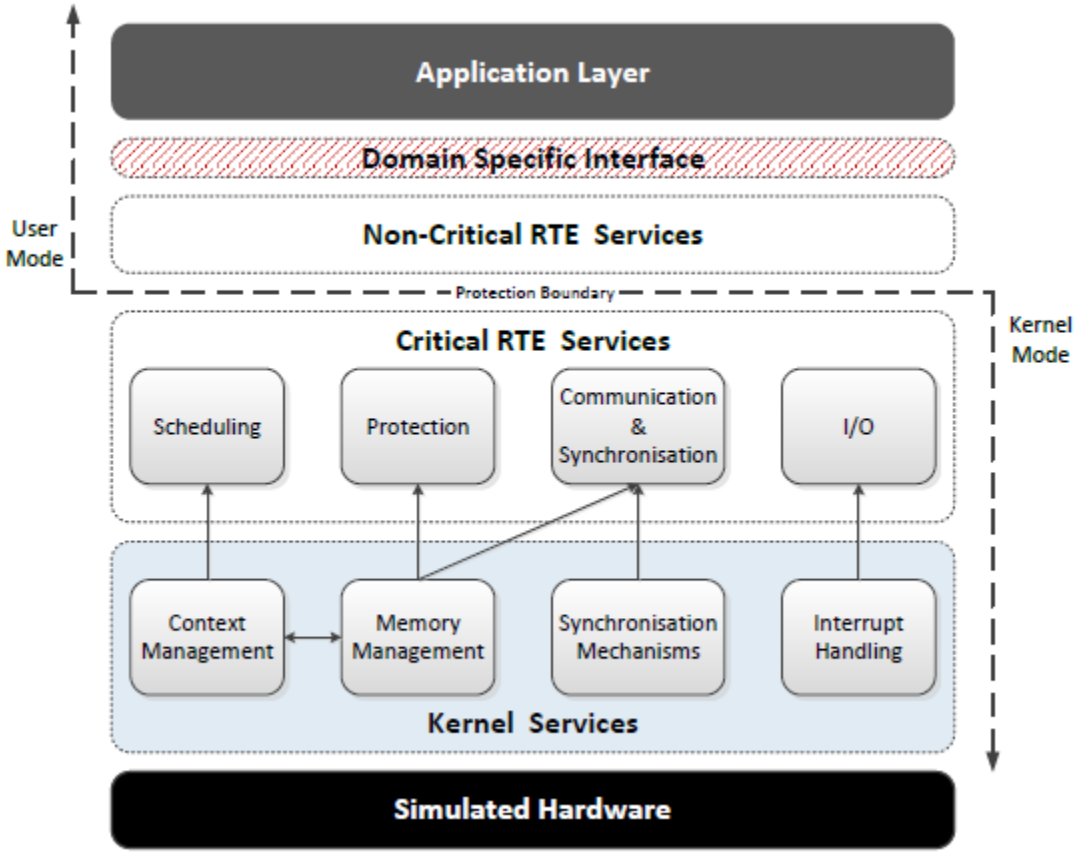
- Stereo navigation (Honeywell International s.r.o.)
- 3D path planning (Honeywell International s.r.o.)
- Diesel engine management system (DENSO Automotive Deutschland GmbH)
- Dynamic compaction machine (BAUER Maschinen GmbH)



3D path planning: Laplacian multi-grid algorithm parallelised by obstacle map partitioning

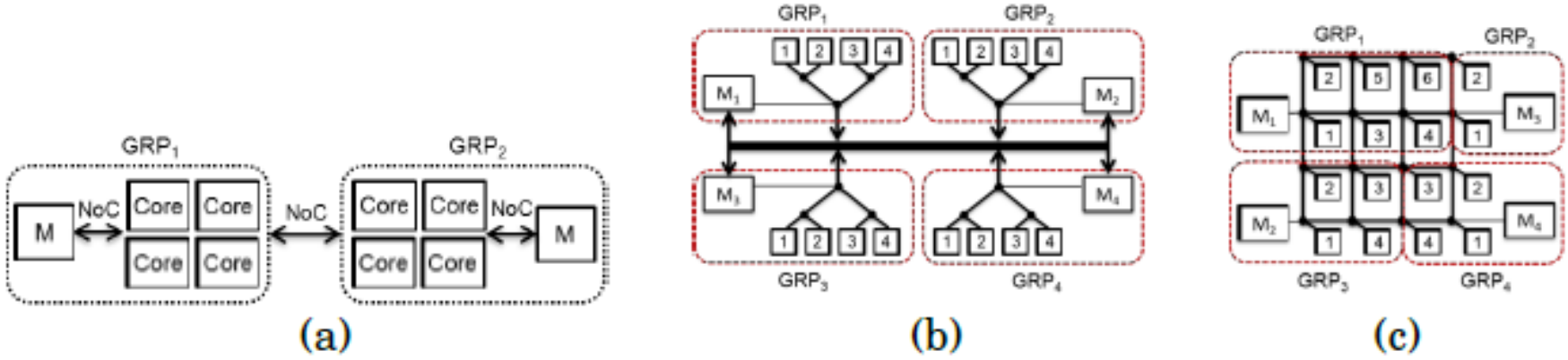
Principal Results (4)

- Hard real-time support in system software
  - Common Kernel Lib
  - Tiny automotive, Tiny avionics, BIOS for crawler crane
  - RTEs



Principal Results (5)

- HW platform: cluster-based multi-core architecture (by BSC)
  Parallel Software Partitions (pSWPs) and
  Guaranteed Resource Partitions (GRPs)
  predictable new cache: ODC^2 (by Tech. Uni. Dortmund)
  all integrated into a single multi-core simulator



- Contributions to AUTOSAR and ARINC Standards and to Open Source Software.

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Results of Parallelisations (1)

$$\textbf{Observed speed-up} = \frac{\text{execution time of the sequential program}}{\text{execution time of the parallelised version}}$$

Execution times measured by parMERASA simulator

$$\textbf{WCET speed-up} = \frac{\text{WCET estimate of the sequential program}}{\text{WCET estimate of the parallelised version}}$$

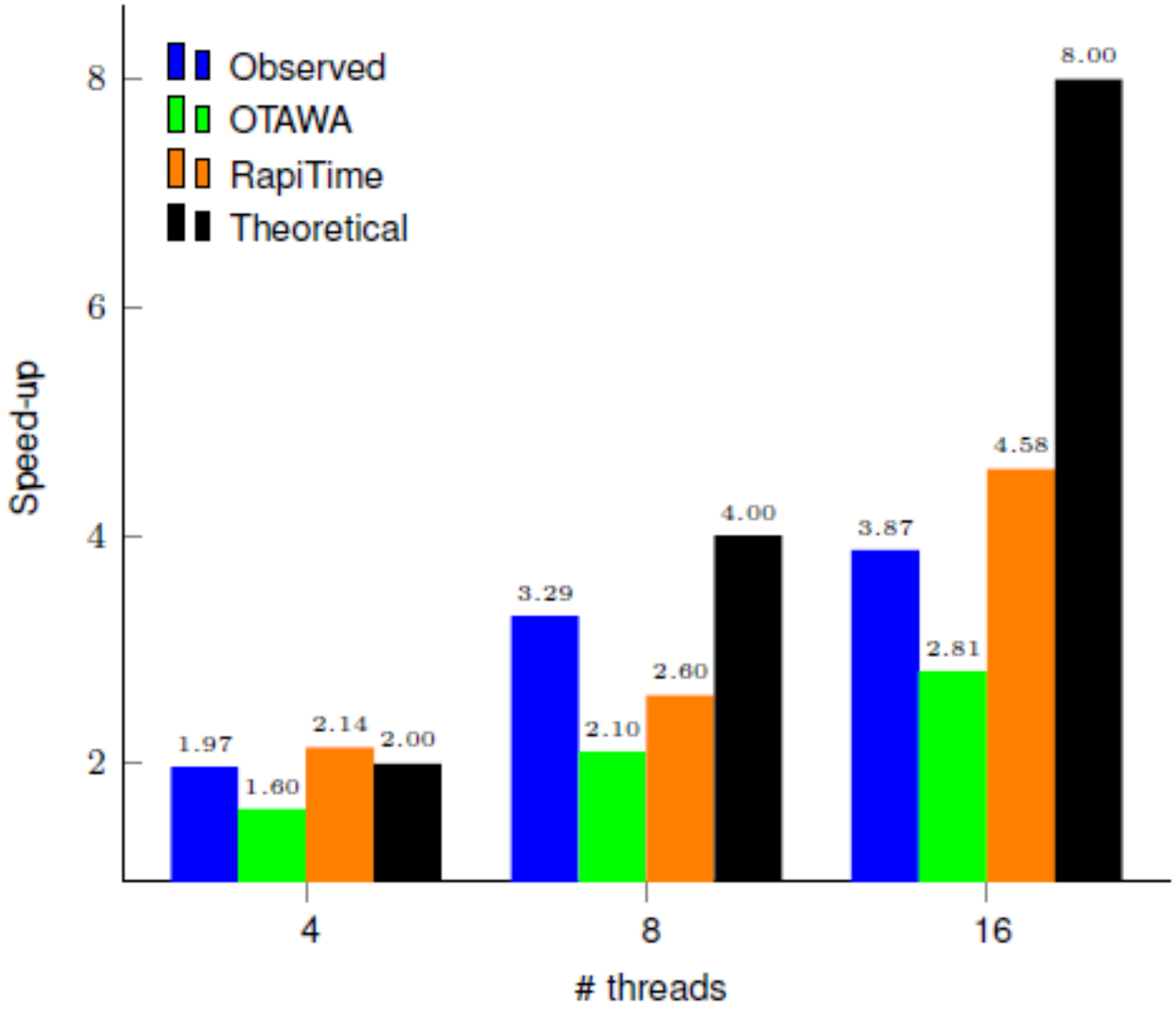
Two types of WCET speed-ups:

based on static WCET bounds reached by OTAWA

based on dynamic WCET estimates based on RapiTime

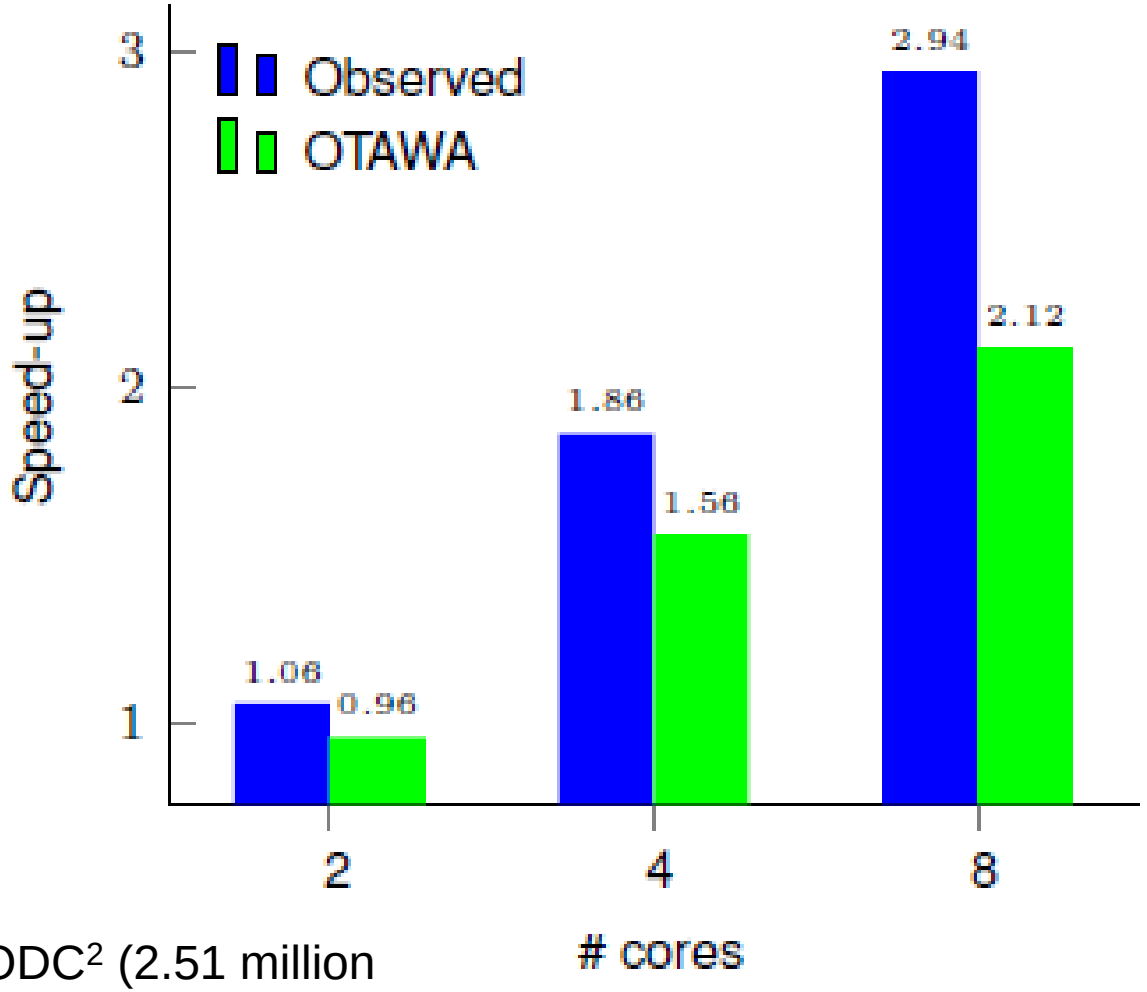
Results of Parallelisations (2)

- **3DPP application** speed-ups with perfect cache coherence



Results of Parallelisations (3)

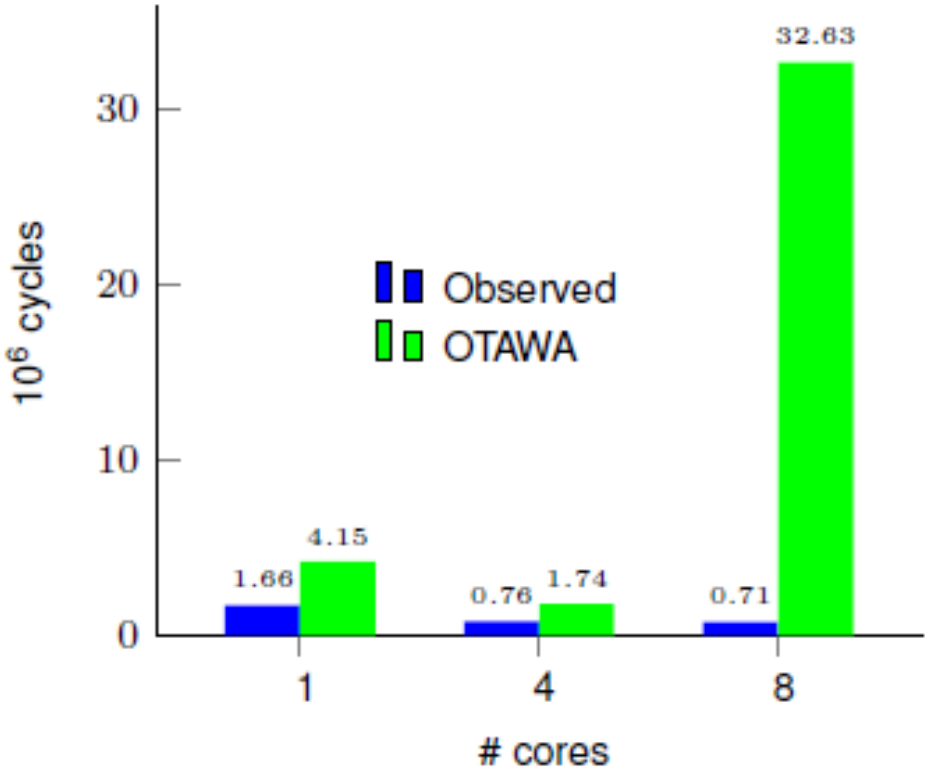
- **3DPP application**
  speed-ups
  with ODC²
  cache coherence

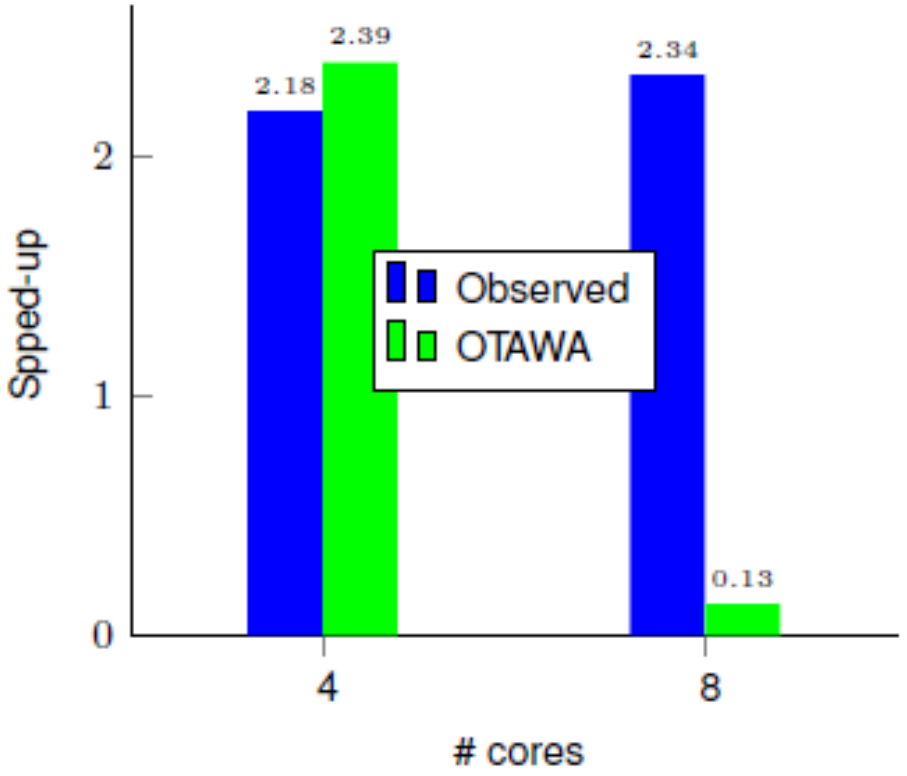


Observed execution time with ODC² (2.51 million cycles) is very close to a cache with perfect coherency protocol (2.42 million cycles for 8 cores)

Results of Parallelisations (4)

- **Compaction machine application**





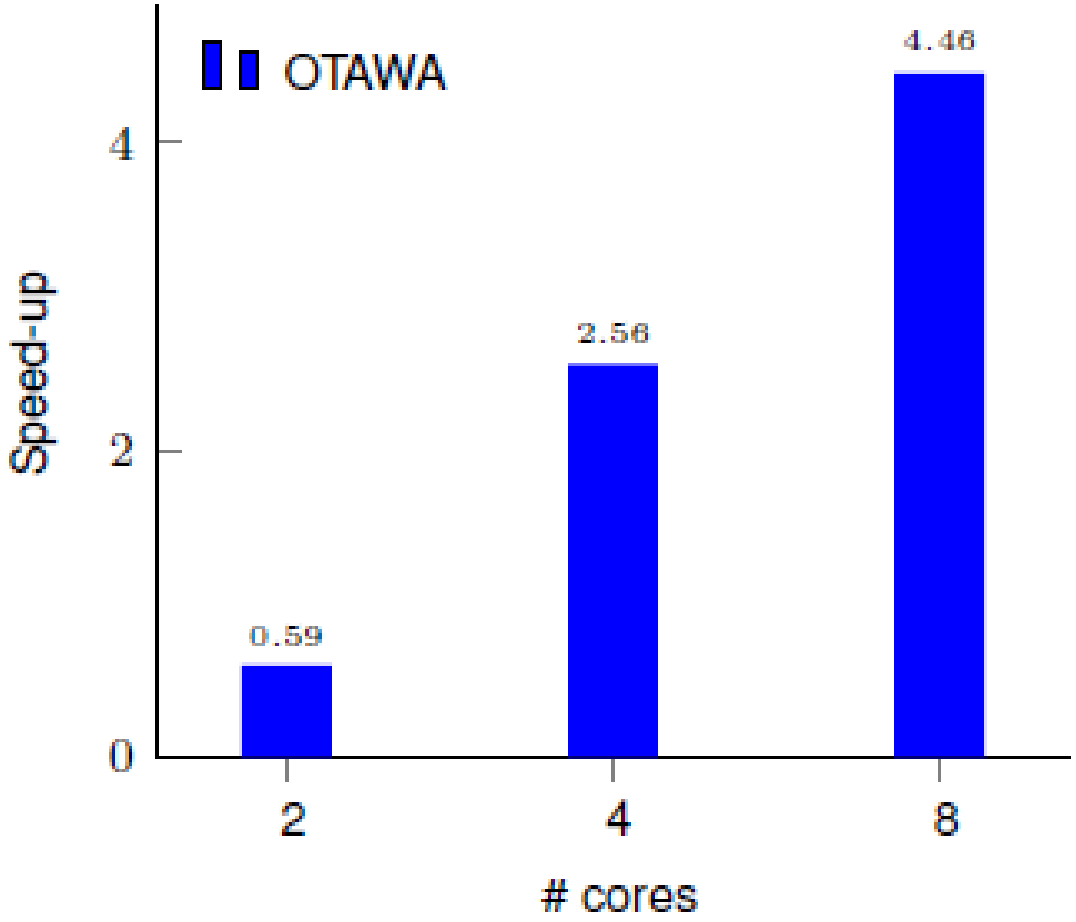
Results of Parallelisations (5)

- **Diesel engine management system**
  1200 runnables
  11 time-driven tasks and
  1 crank-angle task (interrupt from the camshaft sensor)

  (1) Inter-task level: parallel execution of tasks
  (2) Intra-task level: parallel execution of runnables of the same task
  (3) Intra-runnable: parallel execution of instruction blocks or function calls of a runnable.

Results of Parallelisations (6)

- **Diesel engine management system:**
  static WCET speed-up of inter-task parallelization



Results of Parallelisations (6)

- **Diesel engine management system:**
  static WCET speed-up of intra-task parallelization

Task	Sequential	Parallel	Speed-up
τ_1	104260	95845	1.09
τ_4	371453	210032	1.77
τ_5	12426	12426	1.00
τ_8	249165	74842	3.33
τ_{16}	840580	422562	1.99
τ_{20}	65412	32749	2.00
τ_{32}	612863	322600	1.90
τ_{64}	132771	84462	1.57
τ_{96}	102593	82300	1.25
τ_{128}	391206	342665	1.14
τ_{1024}	469303	379605	1.24
τ_{crBas}	833225	437248	1.91

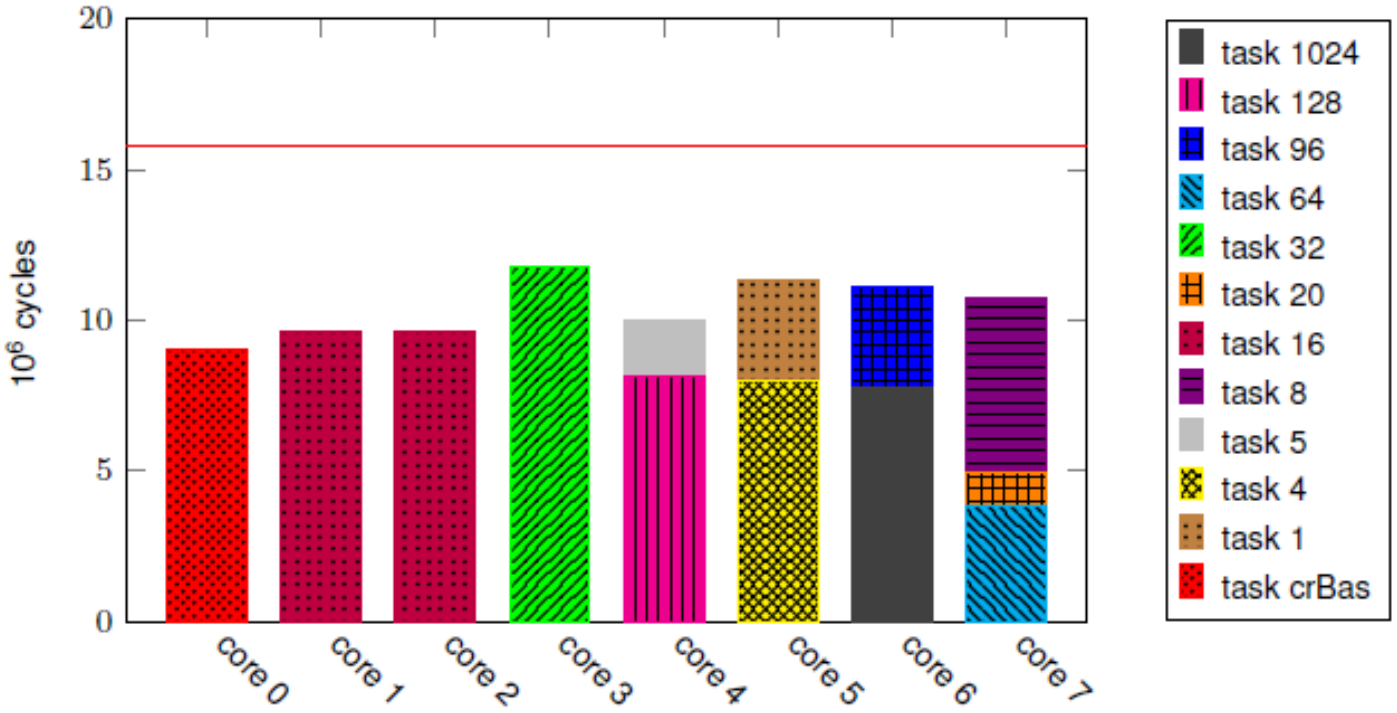
Results of Parallelisations (7)

Diesel engine management system:

Intra- and inter-task parallelism were combined.

Longest running task was distributed over 2 cores.

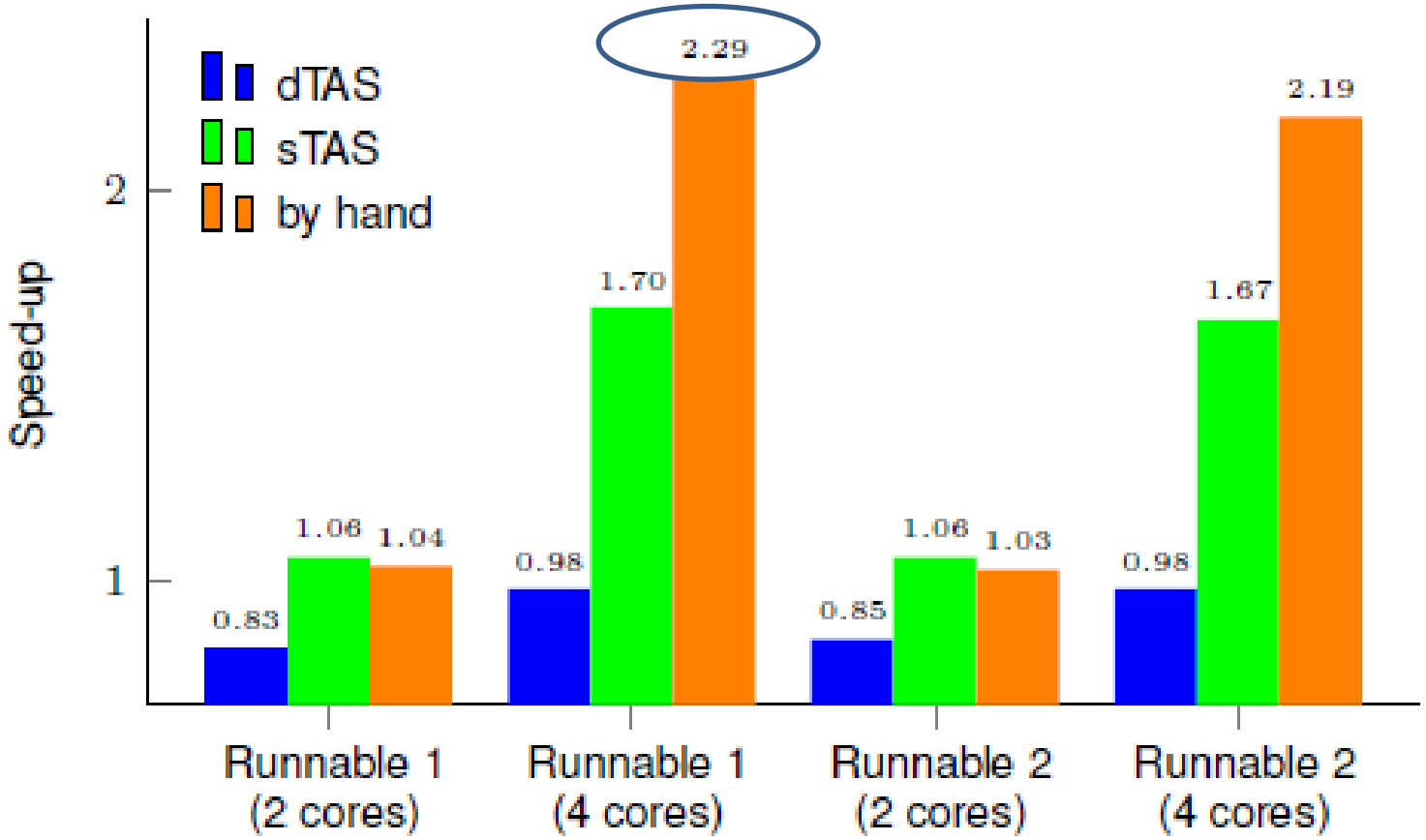
Static WCET speedup estimate increased to **5.97 on 8 cores**.



per core task allocation with combined parallelization approach

Results of Parallelisations (8)

- **Diesel engine management system:** measurement-based WCET speed-up of intra-runnable parallel.



Conclusions

- EC FP-7 parMERASA project (Oct. 1, 2011 - Sept. 30, 2014) targeted future complex control algorithms by parallelizing hard real-time programs.
- Reasonable WCET speed-ups can be reached with a low number of cores, e.g. 5.97 on 8 cores for diesel EMS.
- Scalability of real-world hard real-time applications that run successful on single-core is limited.
- Static WCET speed-ups are limited for high core numbers due to pessimism caused by potentially conflicting global memory accesses in a multi-core.
- parMERASA project paved the way for future high-performance embedded systems applications.
  More complex control algorithms than today can be applied.
  Such algorithms should be designed scalable.

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