On Routing Flexibility of Wormhole-Switched Priority-Preemptive NoCs

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Context & Motivation (1/3)

- Real-Time Systems
  - … where time matters

Bullet dodging in Matrix

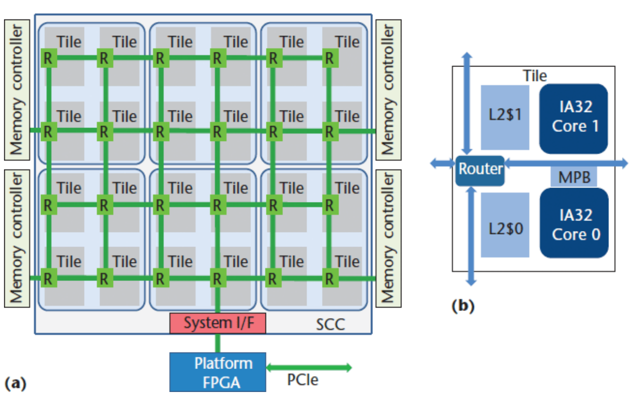
Lance Armstrong “detour”

in Tour de France '03

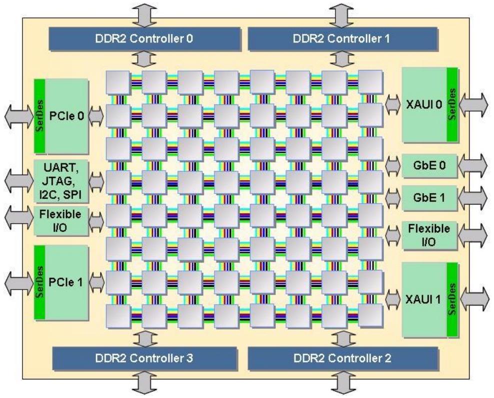
Super Mario video game

Context & Motivation (2/3)

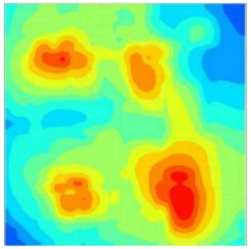
- Multiprocessor platforms

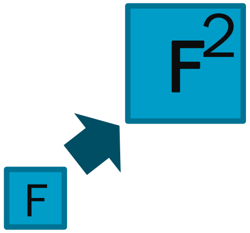


Single-Chip-Cloud Computer (Intel)



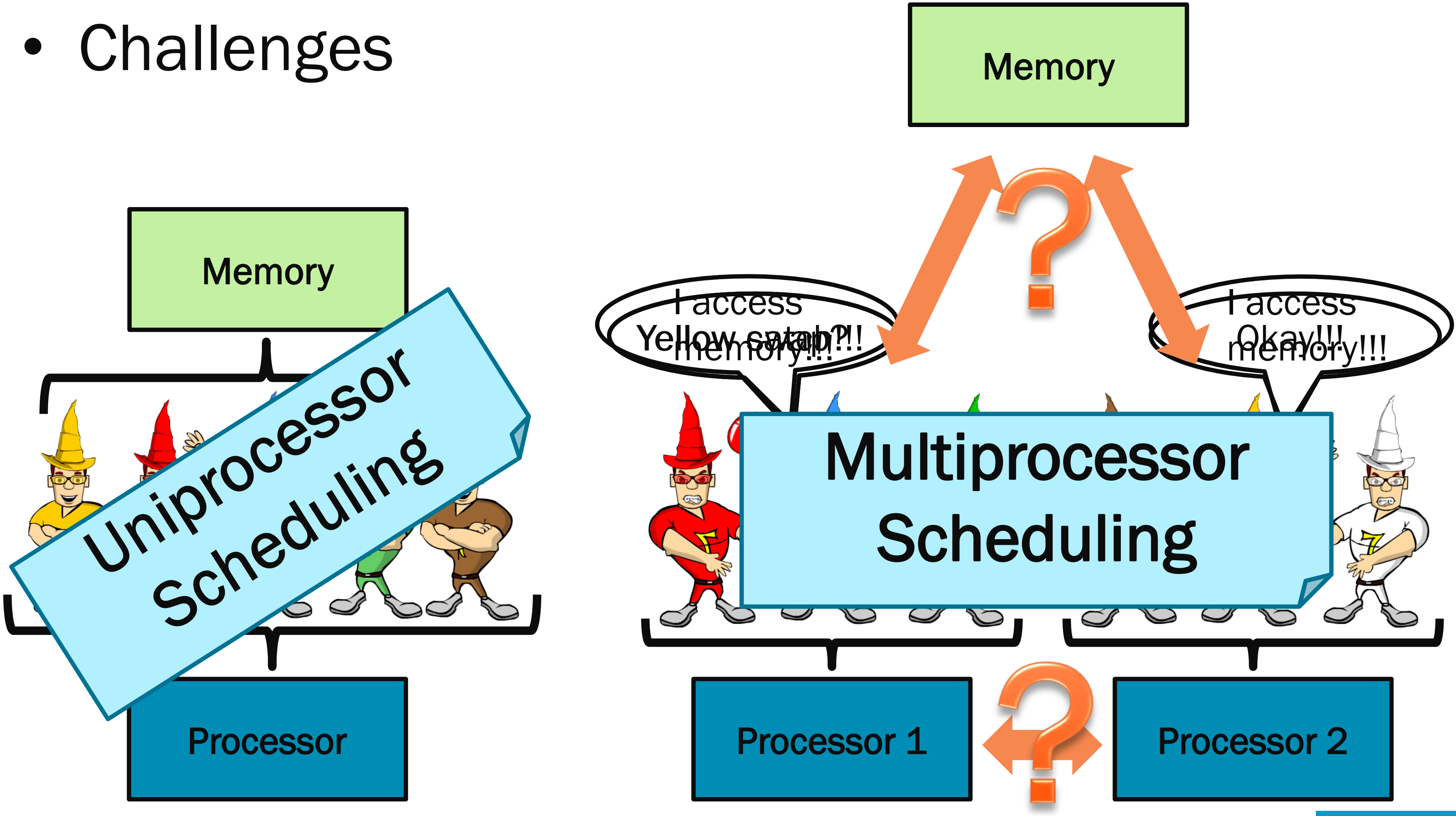
TILEPro64 Processor (Tilera)





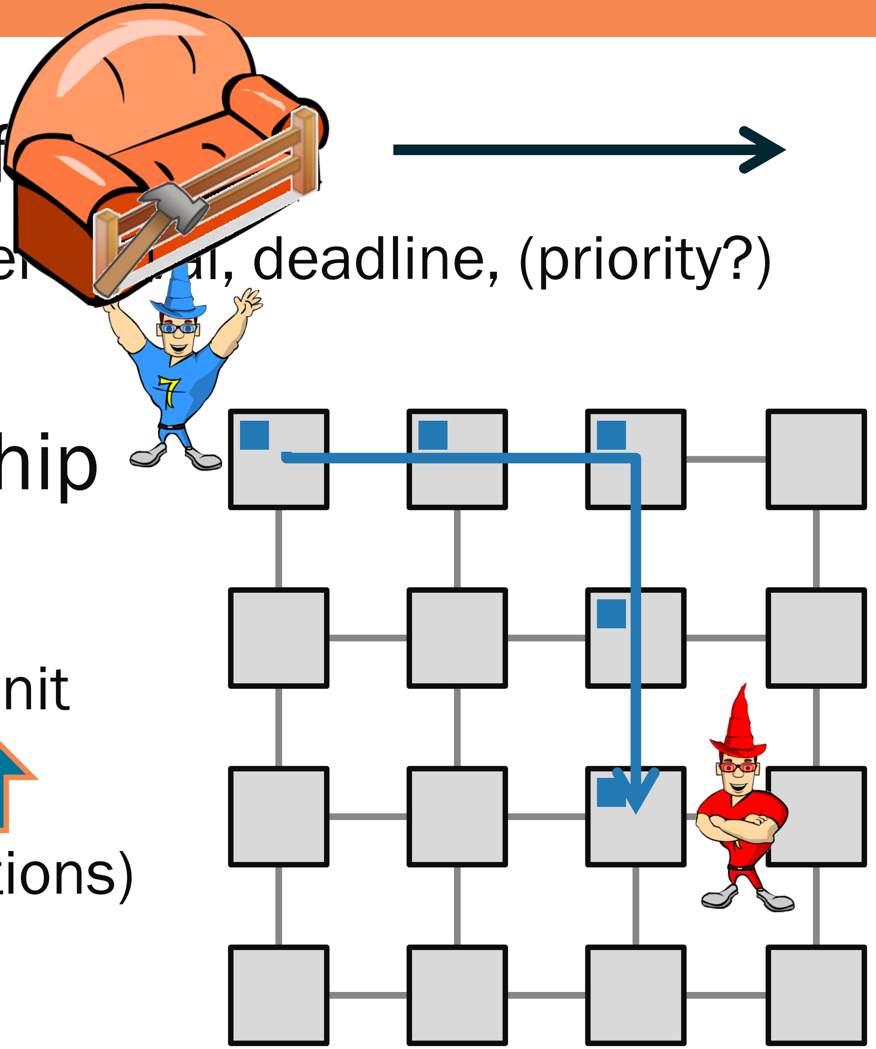
Context & Motivation (3/3)

- Challenges



Model

- Communication => Traff
  - Size, source, destination, inter al, deadline, (priority?)
  - Similar to tasks
- 2-D mesh Network-on-Chip
- Wormhole switching
  - Flit, indivisible transferable unit
  - Throughput/performance
  - Real-time concepts (preemptions)
- Relevant aspects
  - Mapping, routing, (priorities), analysis



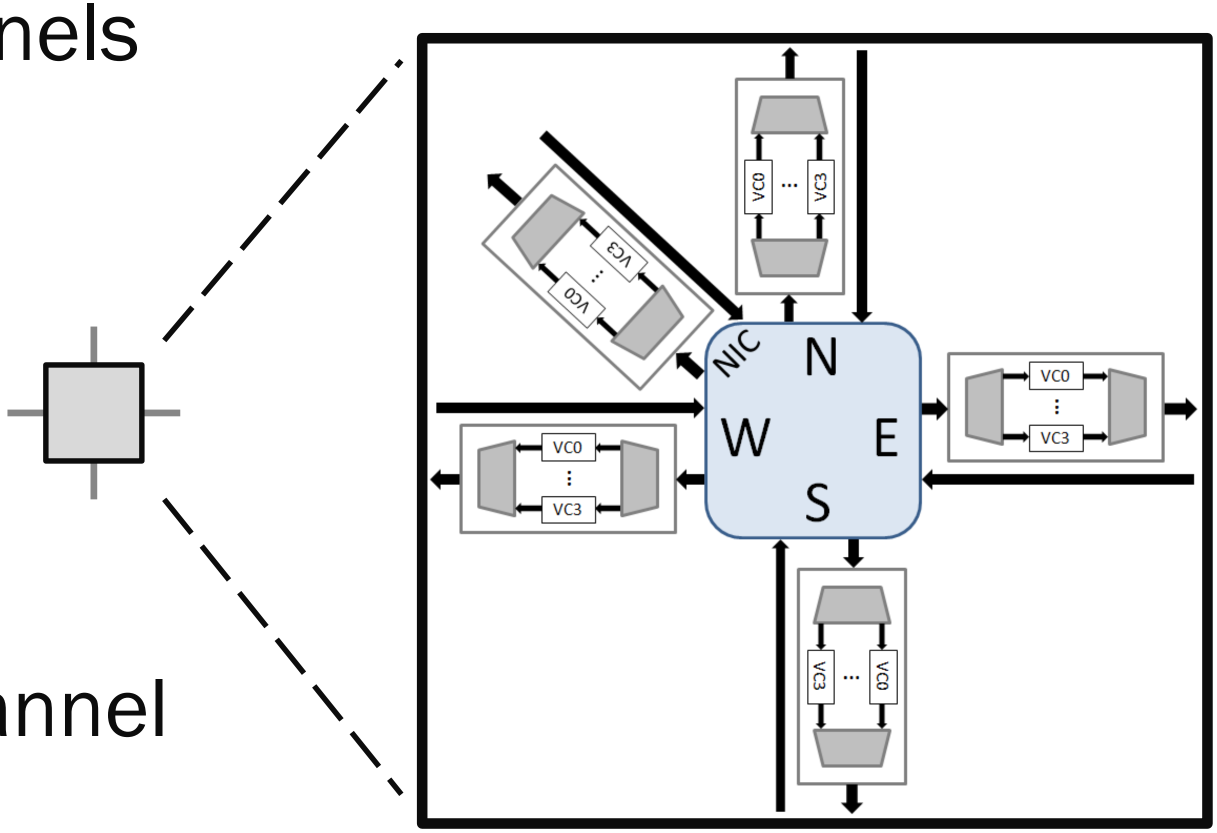
How to implement preemptions?

- Virtual channels

- Buffers

- Flow per channel

- Flit-level preemptions



Related work (1/5)

- Deceptively simple
  - One of the most revisited topics over the last 2 decades

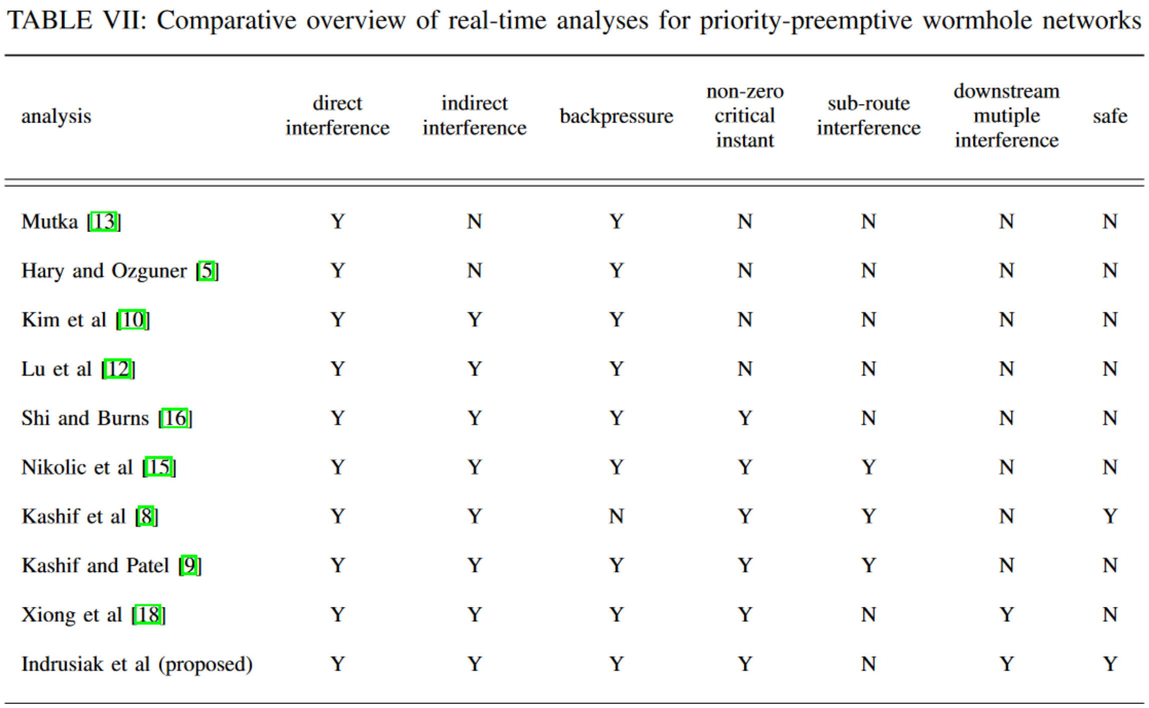


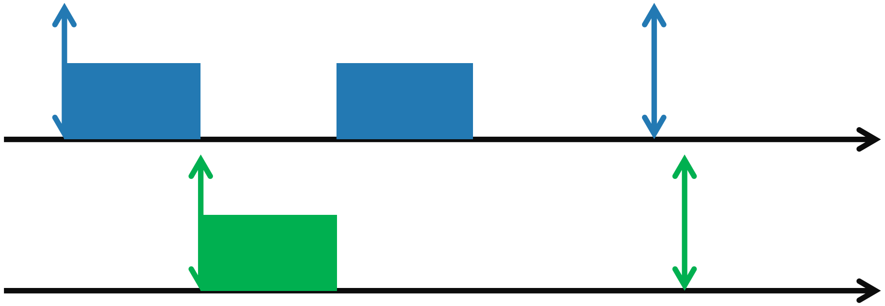
TABLE VII: Comparative overview of real-time analyses for priority-preemptive wormhole networks

analysis	direct interference	indirect interference	backpressure	non-zero critical instant	sub-route interference	downstream mutiple interference	safe
Mutka [13]	Y	N	Y	N	N	N	N
Hary and Ozguner [5]	Y	N	Y	N	N	N	N
Kim et al [10]	Y	Y	Y	N	N	N	N
Lu et al [12]	Y	Y	Y	N	N	N	N
Shi and Burns [16]	Y	Y	Y	Y	N	N	N
Nikolic et al [15]	Y	Y	Y	Y	Y	N	N
Kashif et al [8]	Y	Y	N	Y	Y	N	Y
Kashif and Patel [9]	Y	Y	Y	Y	Y	N	N
Xiong et al [18]	Y	Y	Y	Y	N	Y	N
Indrusiak et al (proposed)	Y	Y	Y	Y	N	Y	Y

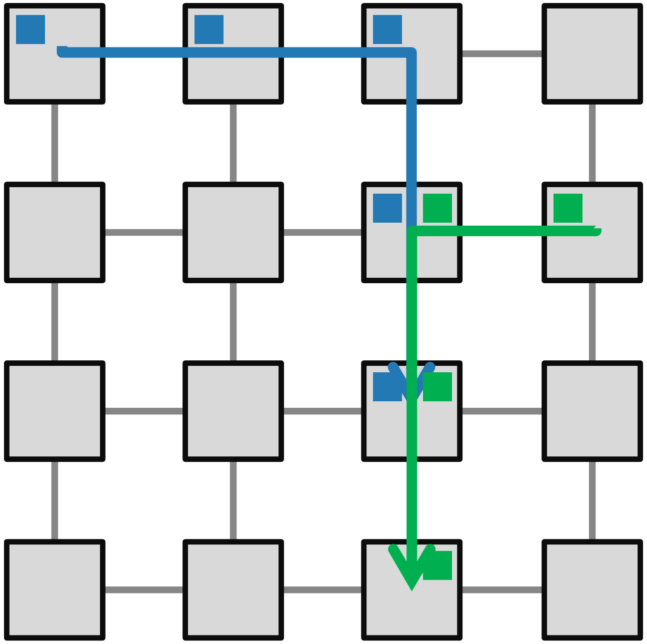
Indrusiak, Burns, Nikolić. **Analysis of buffering effects on hard real-time priority-preemptive wormhole networks.** 2016. arXiv:1606.02942 [cs.NI]

Related work (2/5)

- Preemptions in detail



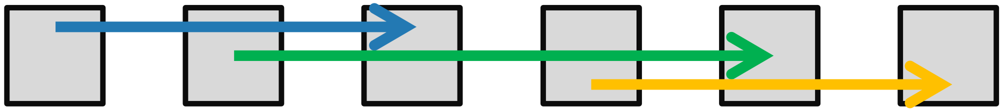
- Not necessary to consider entire paths



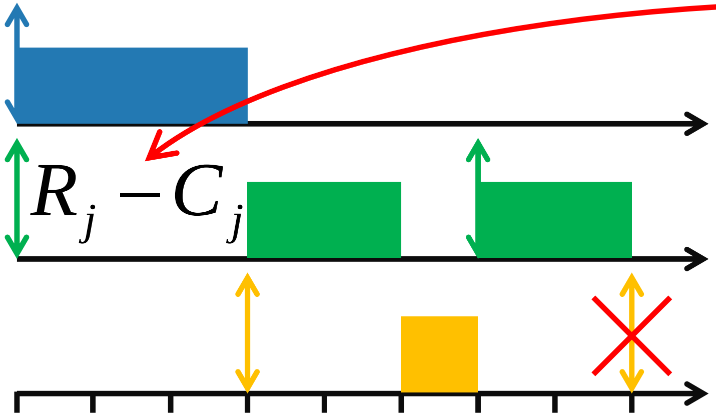
- Max "*per hit*" interference equal to [traversal time – ε]

Related work (3/5)

- Worst-case traversal time: $R_i = C_i + \sum_{\forall f_j \in hp(f_i)} \left\lceil \frac{R_i}{T_j} \right\rceil \times C_j$



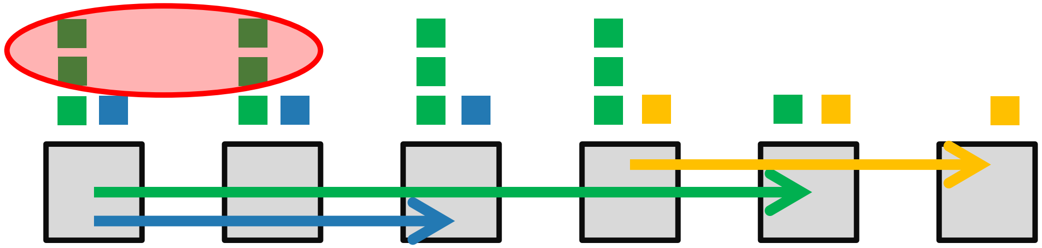
Flow	Priority	C	D = T	R	
f_b	1	3	10	3	✓
f_g	2	2	6	5	✓
f_y	3	2	5	4	✓



$$R_i = C_i + \sum_{\forall f_j \in hp(f_i)} \left\lceil \frac{R_i + J_j}{T_j} \right\rceil \times C_j$$

Shi, Burns. **Real-Time Communication Analysis for On-Chip Networks with Wormhole Switching.** NOCS 2008

Related work (4/5)



Active flows:

τ_1 τ_2 τ_3

- Noticed by Xiong et al.*
  - Implies limited applicability of Shi&Burns analysis
  - But failed to provide safe bounds
- Indrusiak et al.^ proposed the analysis
  - Current state-of-the-art

* Xiong, Lu, Wu, Xie. **Real-Time Analysis for Wormhole NoC: Revisited and Revised.** In GLSVLSI 2016

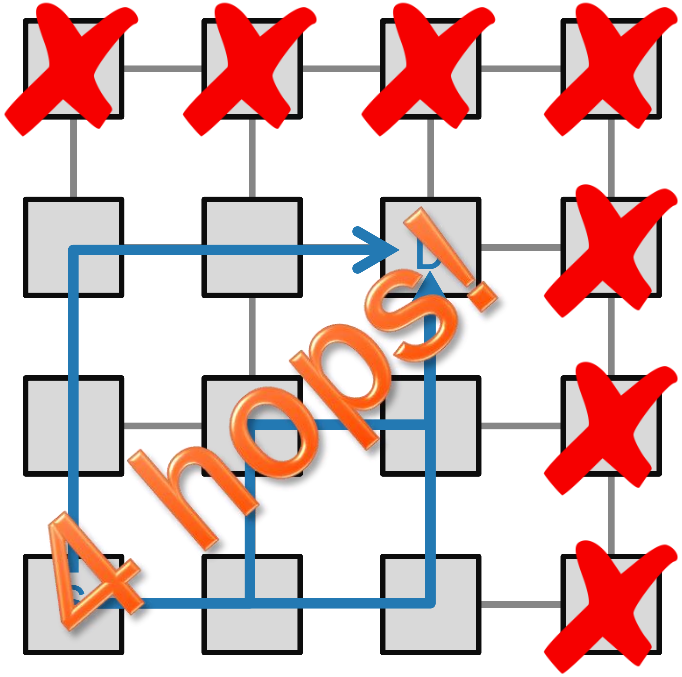
^ Indrusiak, Burns, Nikolić. **Analysis of buffering effects on hard real-time priority-preemptive wormhole networks.** 2016. arXiv:1606.02942 [cs.NI]

Related work (5/5)

- Other investigated aspects
  - Arbitrary deadlines
  - Shared virtual channels
  - Reduced hardware requirements ✓
  - Mapping ✓
  - Priority assignment
  - Arbitration policies ✓
  - Analysis improvements ✓
- What about routing?

Proposed approach (1/5)

- Minimal routes
  - Constant isolation latencies
  - Solution space reduction
  - Paths can be described as:
    - {0, 0, 1, 1}
    - {1, 1, 0, 0}
    - {0, 1, 0, 1}
  - Paths stored in headers
  - #Paths $E_i = \frac{s_i!}{h_i! \cdot v_i!}, \quad s_i = h_i + v_i$
  - No deadlocks



Proposed approach (2/5)

- WCRT depends on hp

$$R_i = C_i + \sum_{\forall f_j \in hp(f_i)} \left\lceil \frac{R_i + J_j}{T_j} \right\rceil \times C_j$$

  – But also depends on priority ordering!

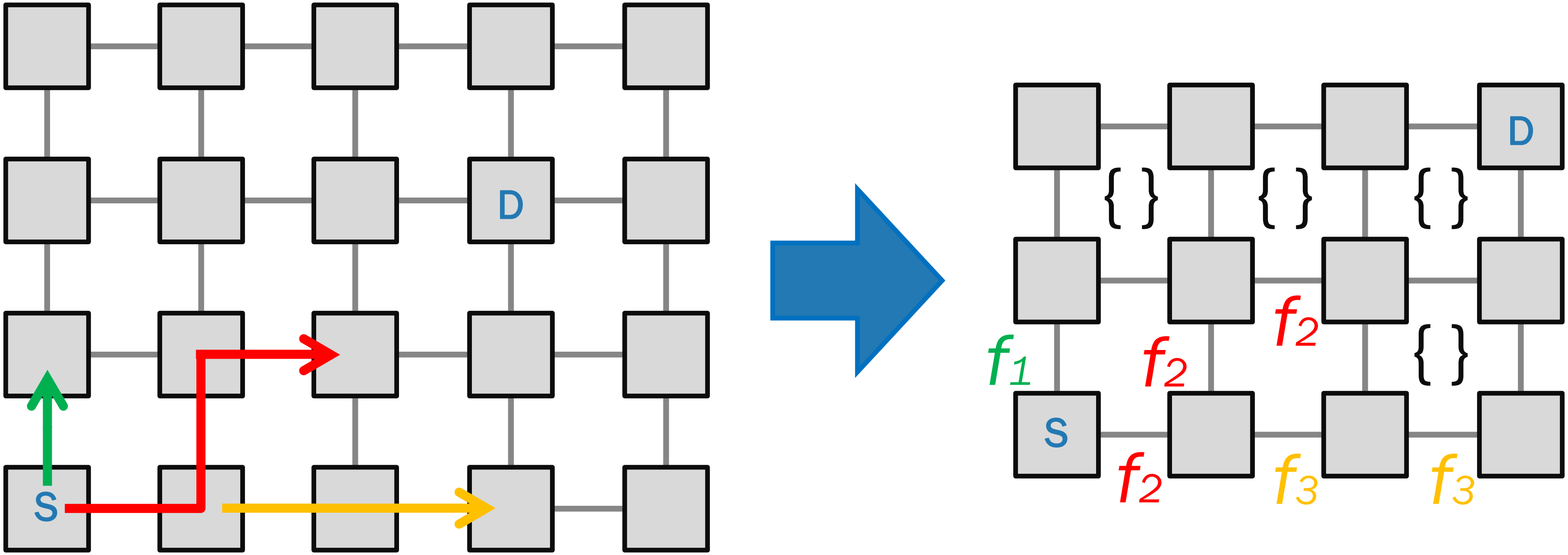
- WCRT not suitable to test candidates
- We introduce Indicative Traversal Time (ITT)

$$R_i^* = C_i + \sum_{\forall f_j \in path(f_i)} \left\lceil \frac{R_i^*}{T_j} \right\rceil \times C_j$$

- Easy to compute
- Generic (not priority dependant)
- Good indication

Proposed approach (3/5)

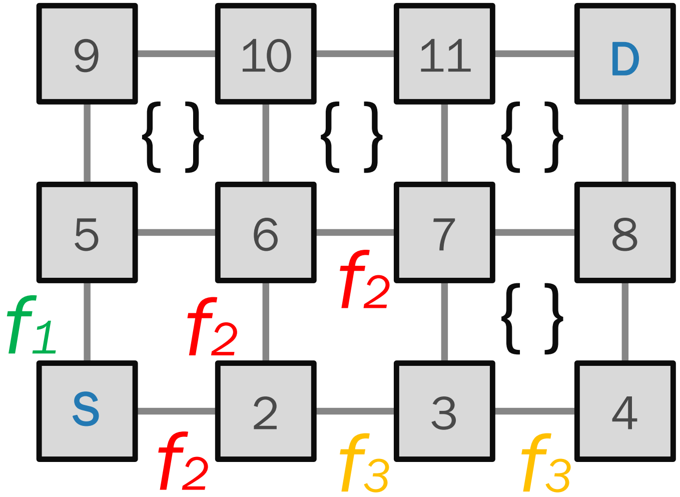
- Find the path with the smallest ITT



- Unfortunately, local minima may not lead to global minima (example of *f1* and *f2*)
- Therefore, Dijkstra’s algorithm does not apply

Proposed approach (4/5)

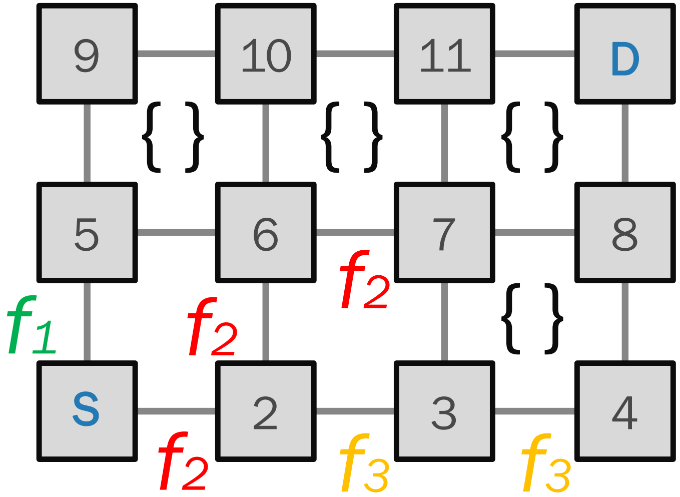
- Construct a table



Step	Path	ITT

Proposed approach (4/5)

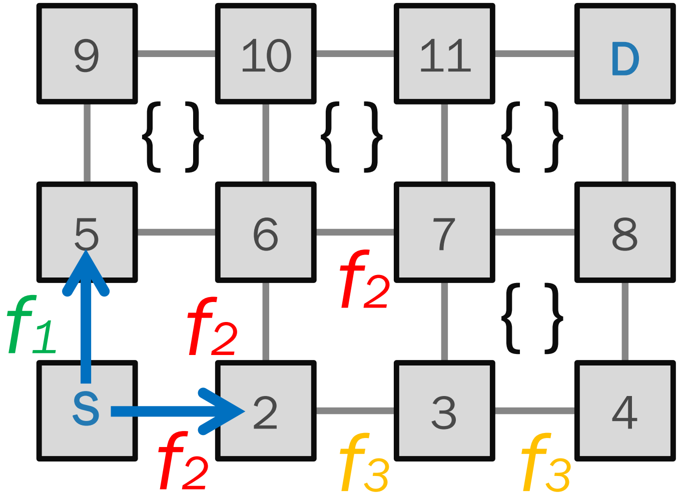
- Construct a table



Step	Path	ITT
1	$\{\rho_1\}$	10

Proposed approach (4/5)

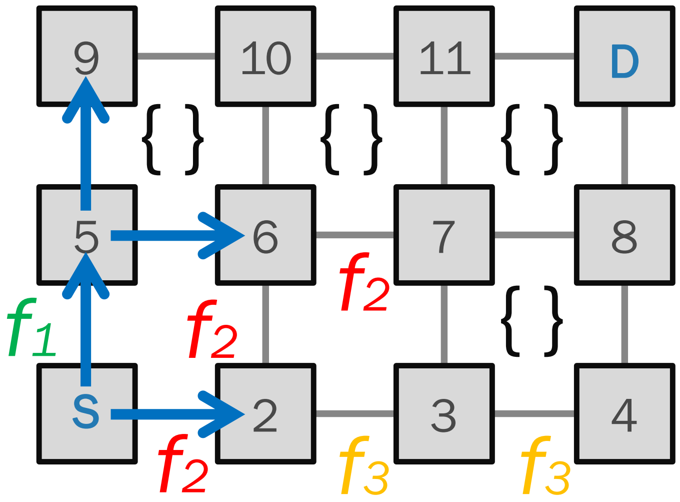
- Construct a table



Step	Path	ITT
1	{ρ1}	10
2	{ρ1, ρ2}	20
	{ρ1, ρ5}	15

Proposed approach (4/5)

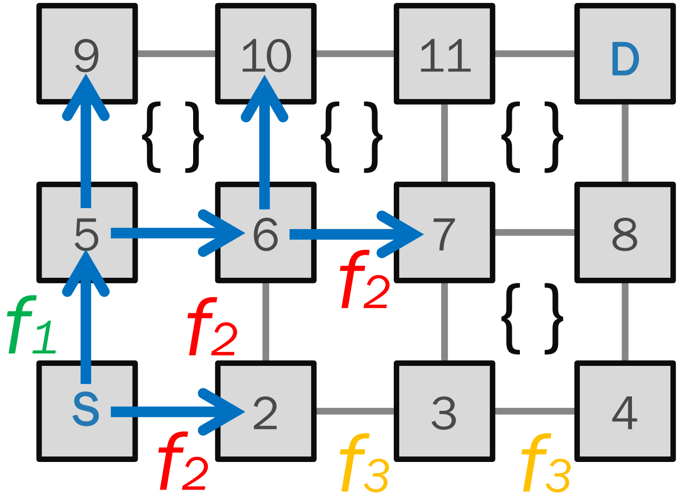
- Construct a table



Step	Path	ITT
1	{ρ1}	10
2	{ρ1, ρ2}	20
	{ρ1, ρ5}	15
3	{ρ1, ρ2}	20
	{ρ1, ρ5, ρ6}	15
	{ρ1, ρ5, ρ9}	15

Proposed approach (4/5)

- Construct a table



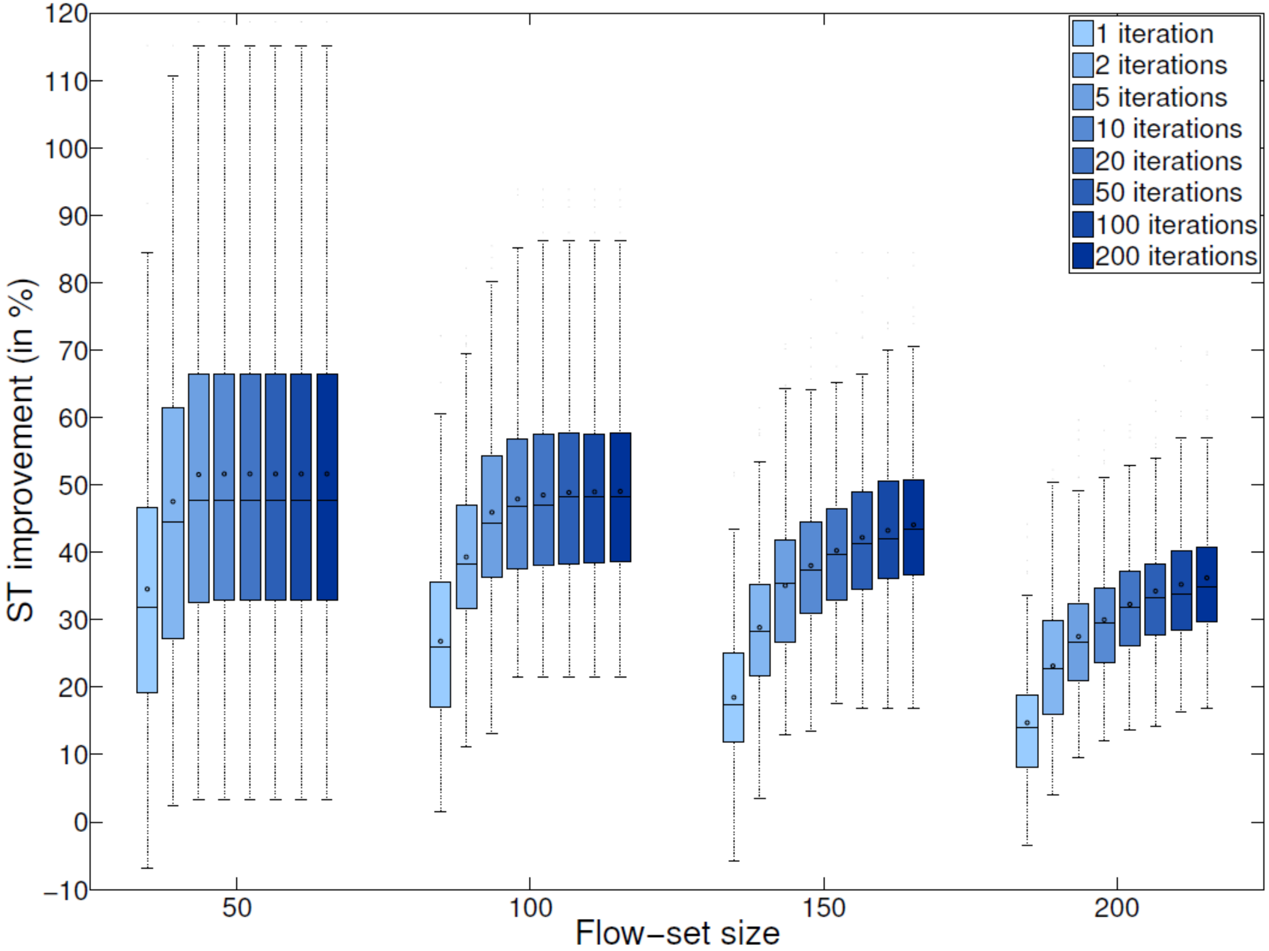
Step	Path	ITT
1	{ρ1}	10
2	{ρ1, ρ2}	20
	{ρ1, ρ5}	15
3	{ρ1, ρ2}	20
	{ρ1, ρ5, ρ6}	15
	{ρ1, ρ5, ρ9}	15
4	{ρ1, ρ2}	20
	{ρ1, ρ5, ρ6, ρ7}	25
	{ρ1, ρ5, ρ6, ρ10}	15
	{ρ1, ρ5, ρ9}	15

Proposed approach (5/5)

- Compute #paths for all flows
- Sort non-decreasingly and treat in that order
- Find and assign a minimal path with min ITT
- After all paths are derived, assign priorities
- If schedulable => success
- If not, invoke path derivation & priority assignment again
- Until success
  - Or same paths & priorities => unschedulable

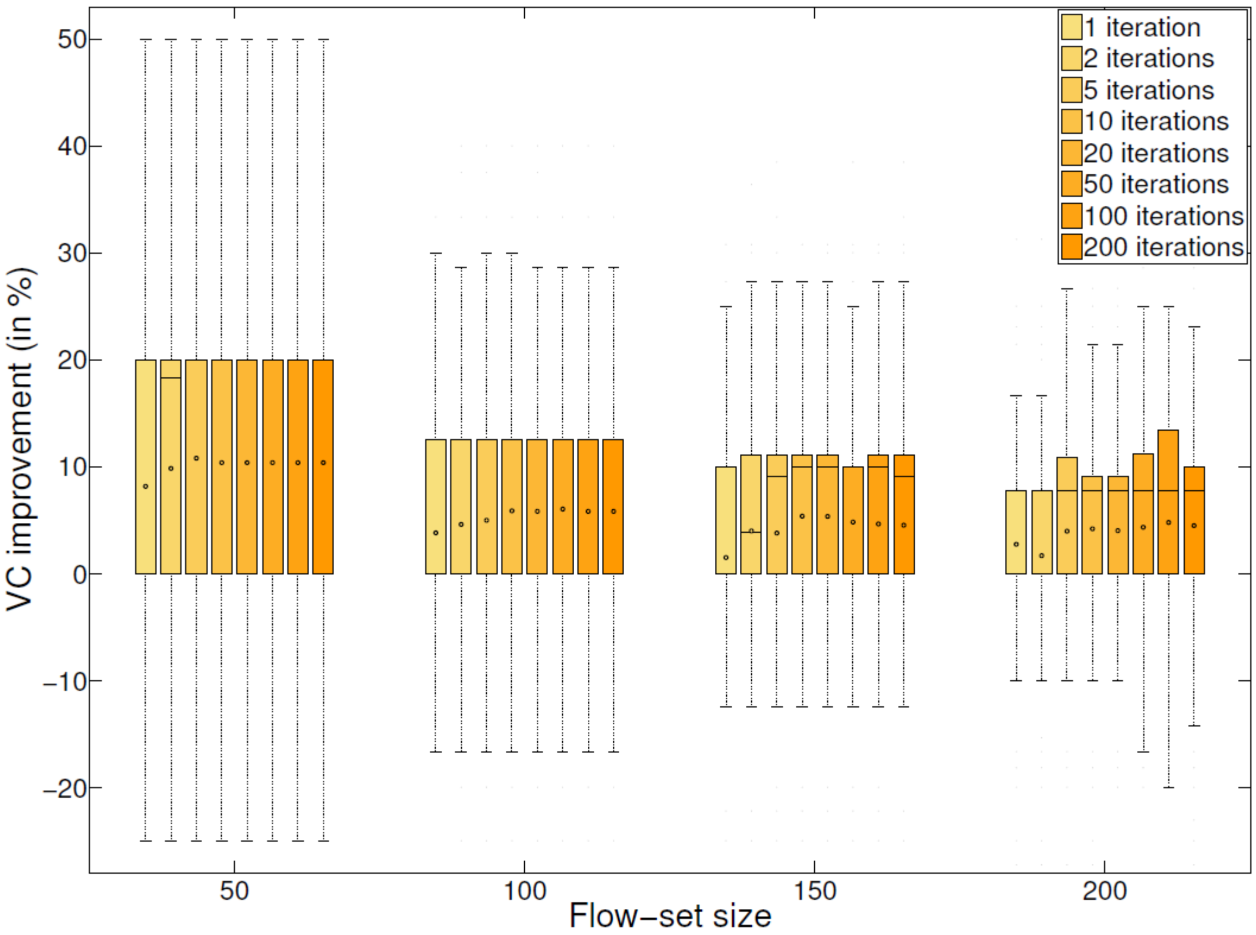
Evaluation (1/5)

- Schedulability improvements over best{XY,YX}



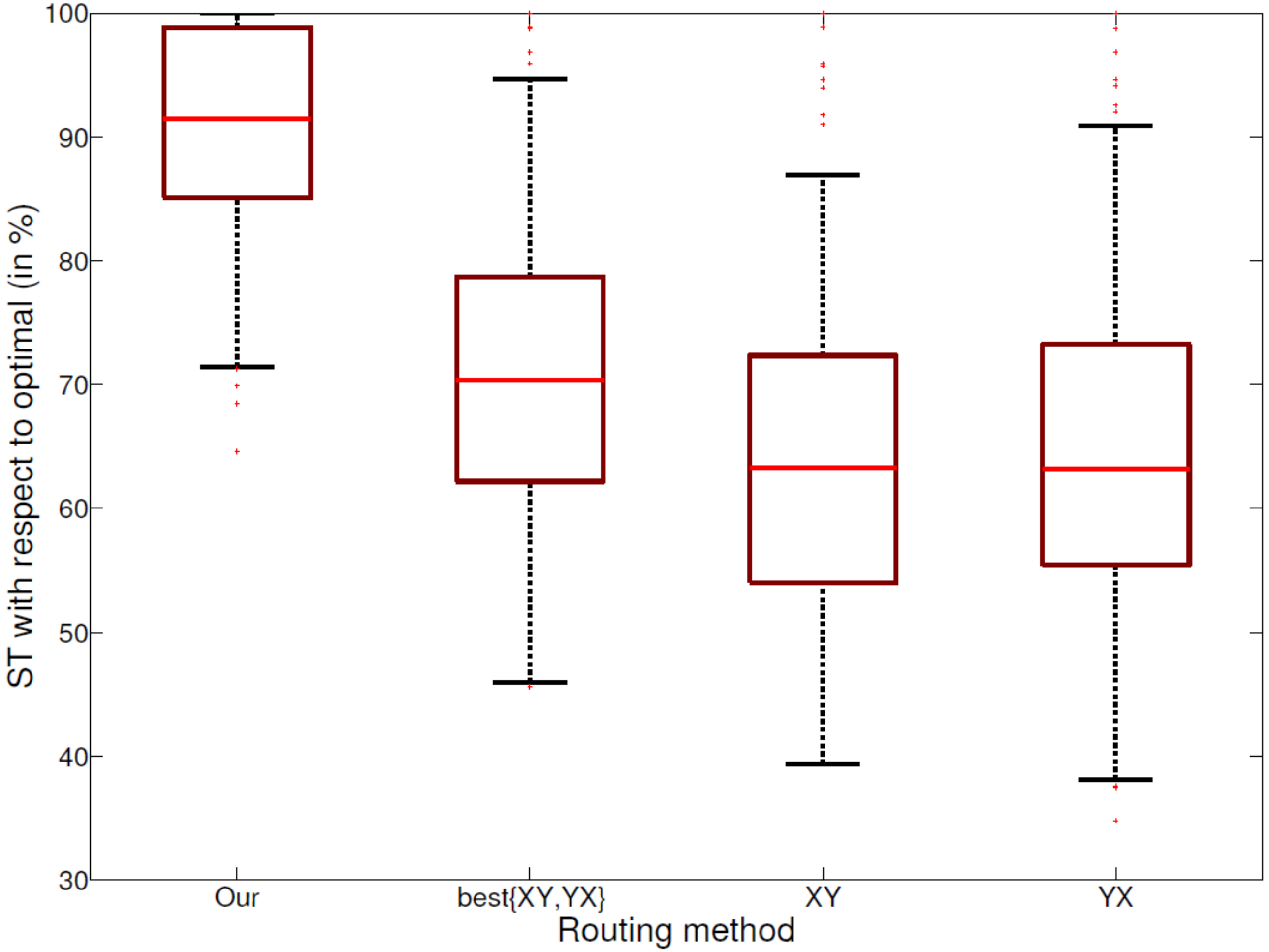
Evaluation (2/5)

- VC improvements over best{XY,YX}



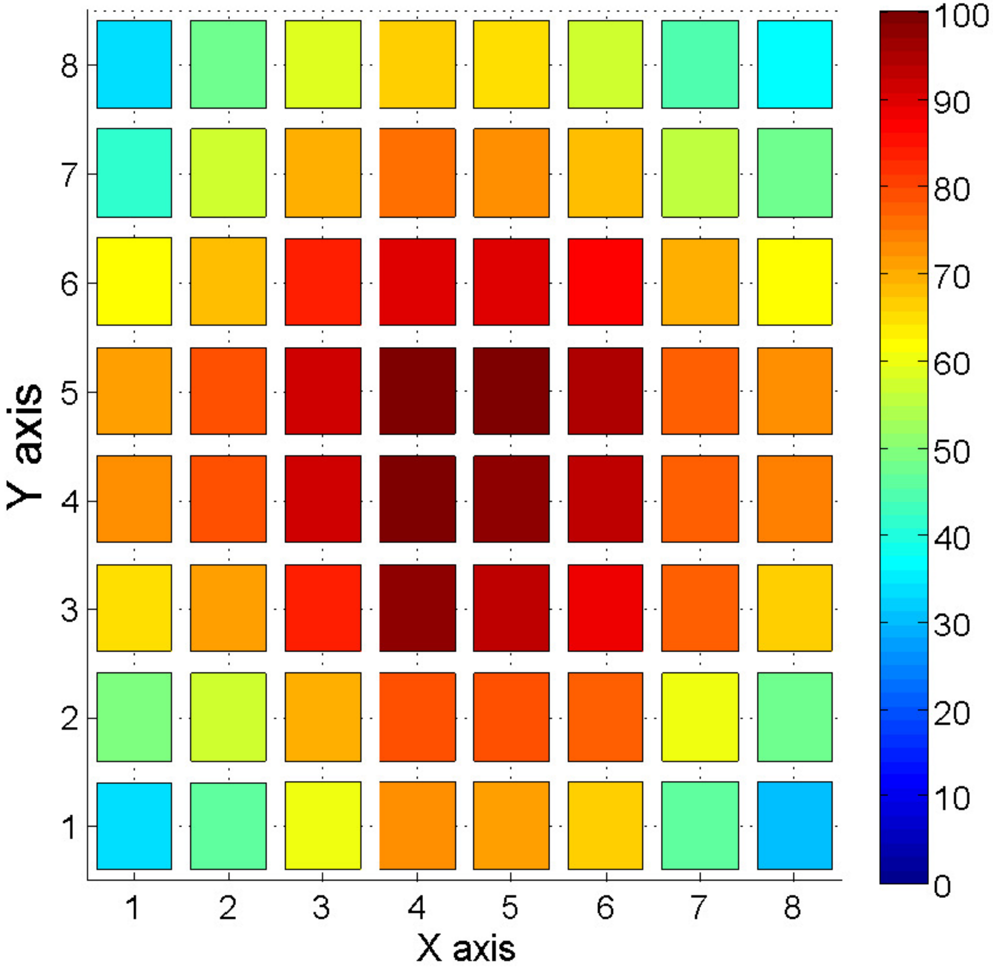
Evaluation (3/5)

- Schedulability w.r.t. optimal



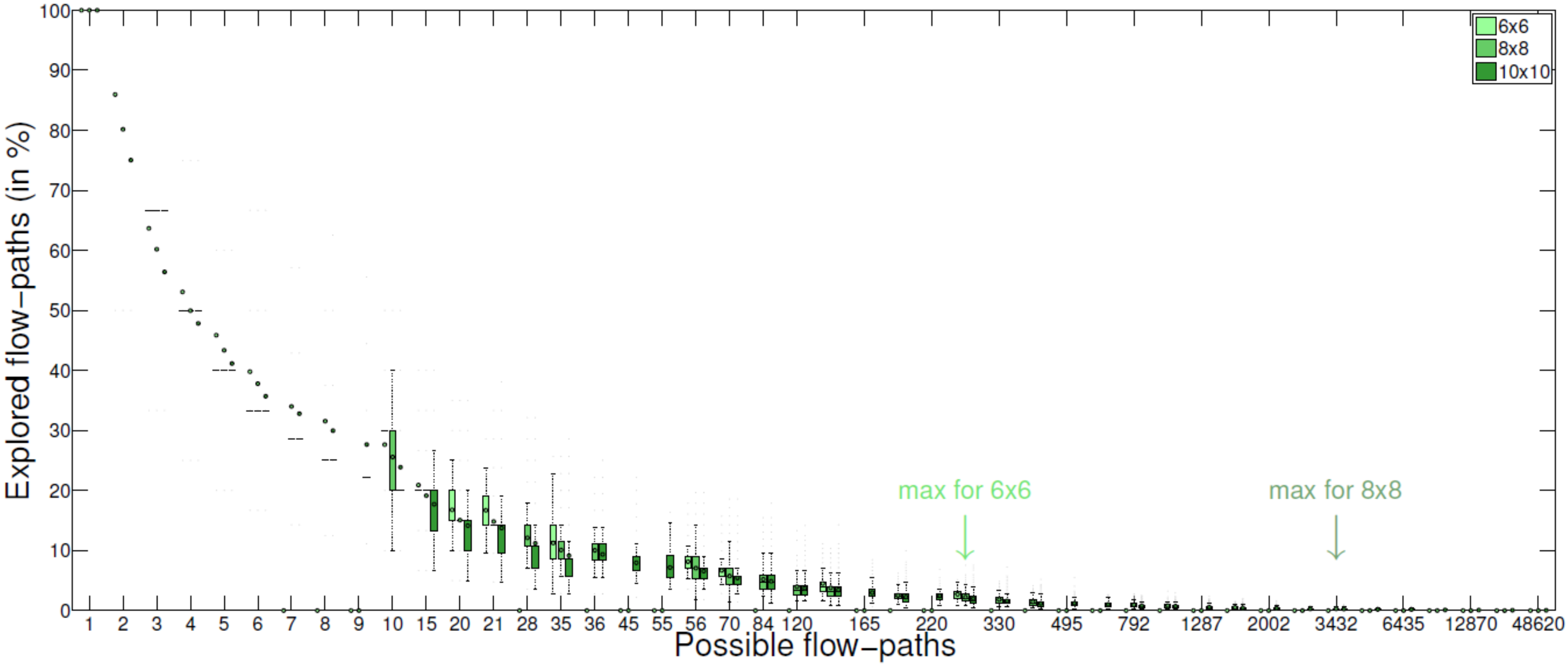
Evaluation (4/5)

- Traffic distribution



Evaluation (5/5)

- Computational complexity

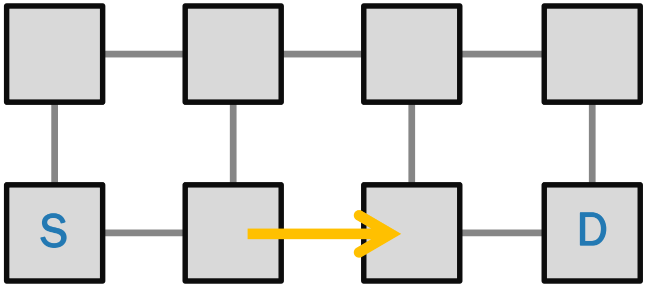


Conclusions

- Dimension-ordered routing not efficient!
- ITT metric suitable for this class of problems
- Minimal routes for search space reduction
- Proposed method
  - Outperforms dimension-ordered routing methods
  - Near optimal on a small-scale example
  - Good workload distribution
  - Scalable

Future work

- Extend to non-minimal paths?
- Optimal routes and priorities?
- How to combine with mapping?



Thank you

Questions?